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# A FUNCTIONAL DESCRIPTION OF THE NAVSTAR GPS RECEIVER MODEL X

FINAL REPORT FOR
SAMSO CONTRACT F04701-75-C-0212
VOLUME I

by
William M. Stonestreet

26 April 1976
Revised February 1977



The Charles Stark Draper Laboratory, Inc.
Cambridge, Massachusetts 02139

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The material presented is considered to be an accurate representation and/or resolution of sometimes conflicting information gathered from the cited sources. It is recognized that the design of the X-Receiver is still in the process of evolution at Magnavox APD and that certain parts of the description may have to be modified to reflect the latest design decisions and/or to correct any misunderstandings that may exist.

The author wishes to thank Dr. Duncan B. Cox, Jr., and Dr. Bernard A. Kriegsman who participated in the interviews at the JPO, for their assistance in formulating the technical concepts and in reviewing the text.

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Draper Laboratory is under contract to the Global Positioning System (GPS) Joint Program Office (JPO) to develop the interface requirements between the GPS X-set being developed by Magnavox Advanced Product Division under subcontract to General Dynamics and the Advanced Inertial Reference System (AIRS). Since the X-set is still under development, a suitable description of it must be created in order to develop this interface. With the exception of the data processor and the X-receiver calibration and automatic-fault indicator operations, this report functionally describes the operations performed by the X-set.

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20. Abstract (Con't)

The descriptions contained herein are based upon the documentation and specifications currently available and technical discussions with the GPS JPO.

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## Section 1. Introduction

Draper Laboratory is under contract to the Global Positioning System (GPS) Joint Program Office (JPO) to develop the interface requirements between the GPS X-set being developed by Magnavox Advanced Product Division under subcontract to General Dynamics and the Advanced Inertial Reference System (AIRS). Since the X-set is still under development, a suitable description of it must be created in order to develop this interface. With the exception of the data processor and the X-receiver calibration and automatic fault indicator operations, this report functionally describes the operations performed by the X-set. The descriptions contained herein are based upon the documentation and specifications [1,2,3,4]* currently available and technical discussions with the GPS JPO [5,6,7,8].

*Numerals in brackets refer to similarly numbered references in the List of References, Section 19.

## Section 2. X-Set User Equipment

A functional block diagram of the X-set is shown in Figure 1. The set consists of two antennas, the X-receiver, a data processor, control and display unit, and a source of power. Each of the two antennas receives both the L1 and L2 frequencies. The X-receiver acquires the signals, tracks the carriers and codes of either the Precision (P) or Coarse/Acquisition (C/A) signals at either the L1 or L2 frequencies, demodulates incoming data, and measures the pseudo-range and delta range. The data processor selects the satellites to be tracked and performs the navigation processing.

The X-set has the capability of using an internal reference oscillator or an external oscillator as a frequency source and/or an external clock for accurate time-of-week information. The X-set is also able to use data from an Inertial Measurement Unit (IMU) to provide better velocity and position estimates. The IMU data is used in the navigation filter and to provide a carrier estimate when the carrier is lost.

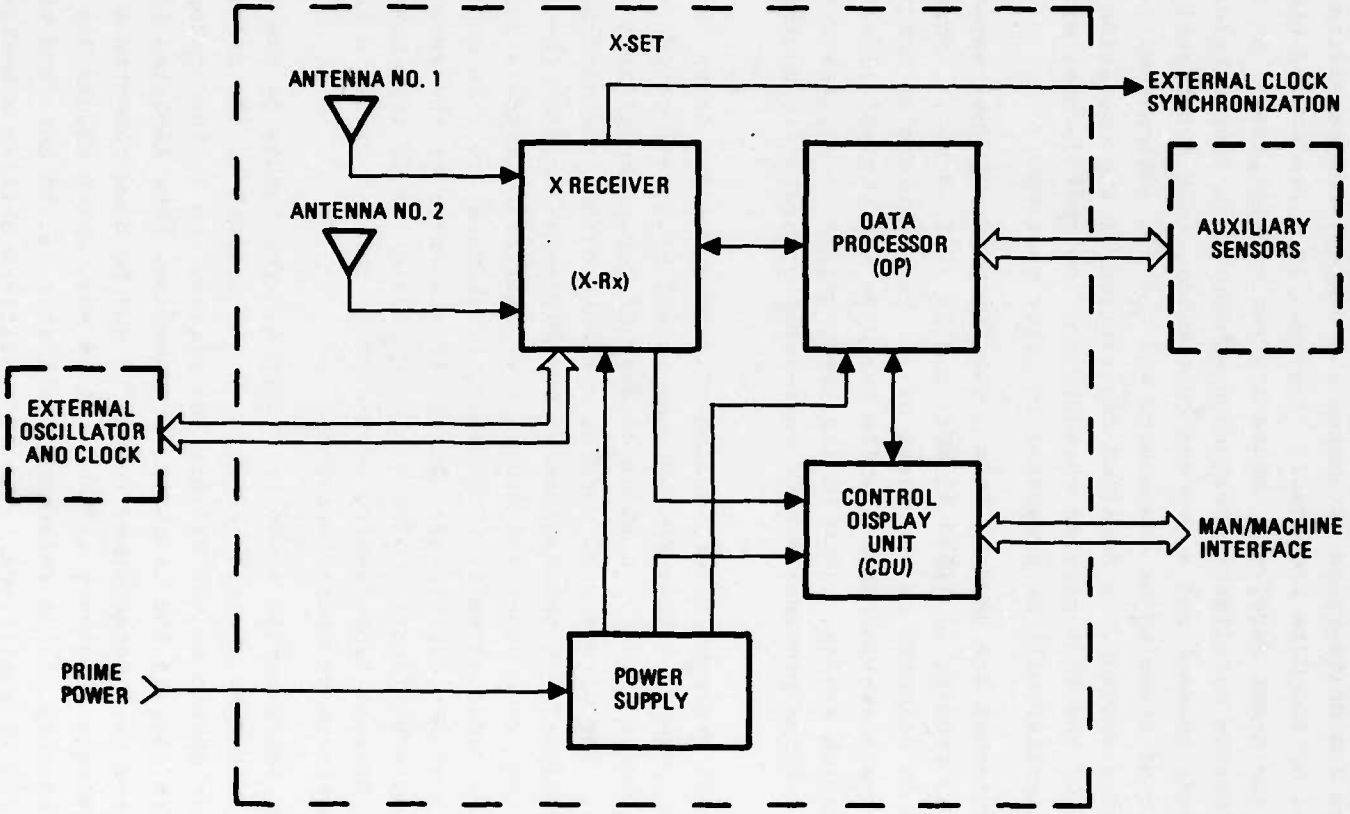



Figure 1. X-Set User Equipment
From Reference [1]

## Section 3. X-Set Receiver

The main objective of the X-set Receiver is to accept as inputs the signals from the two antennas, process them, and provide usable pseudo-range and delta-range estimates and demodulated satellite data as requested by the data processor. Figure 2 is a functional block diagram of the X-set receiver. There are two preamplifiers, an RF converter, reference oscillator, frequency synthesizer, four carrier channels, one code channel and a process controller. The functional operation of each of these major components and the two antennas will be discussed in this section. A detailed description of the operation and interaction of the four carrier channels and the code channel with the process controller will be presented in later sections.

Two antennas are used to form a quasi-omnidirectional antenna. Both antennas receive L1 (1575.42 MHz) and L2 (1227.6 MHz). Normally one antenna is selected on the basis of its beam pattern to track satellites with low elevation angles while the other tracks satellites with higher elevation angles. (Due to its lower gain at low elevation angles the latter antenna provides higher anti-jamming capability against ground jammers).

There is a preamplifier located at each antenna. As an input the preamplifier accepts either the antenna signal or a calibration signal provided by the receiver. A block diagram of the preamplifiers is shown in Figure 3. The directional coupler connects either the antenna or calibration signals to the diplexer. The diplexer isolates the L1 and L2 signals from each other and from other interfering signals such as phase-arrayed radar signals. The L1 and L2 signals are then amplified and summed together for transfer to the RF converter at the receiver. Isolation and amplification of the L1 and L2 signals in this manner prevents these signals from jamming each other. Table 1 presents the preamplifier performance characteristics.

The RF converter is shown in Figure 4. The inputs to the RF converter are either calibration signals or the outputs of the preamplifiers and are chosen by the calibration mixers. As in the preamplifier, the diplexers isolate the L1 and L2 frequencies. The isolated L1 and L2 signals are then heterodyned in the L1 and L2 down converters to the same Intermediate Frequency (IF) of 184.14 MHz, which equals 36F where F is the frequency of the reference oscillator, 5.115 MHz, and then amplified in the IF amplifiers. The IF amplifiers utilize a total-power

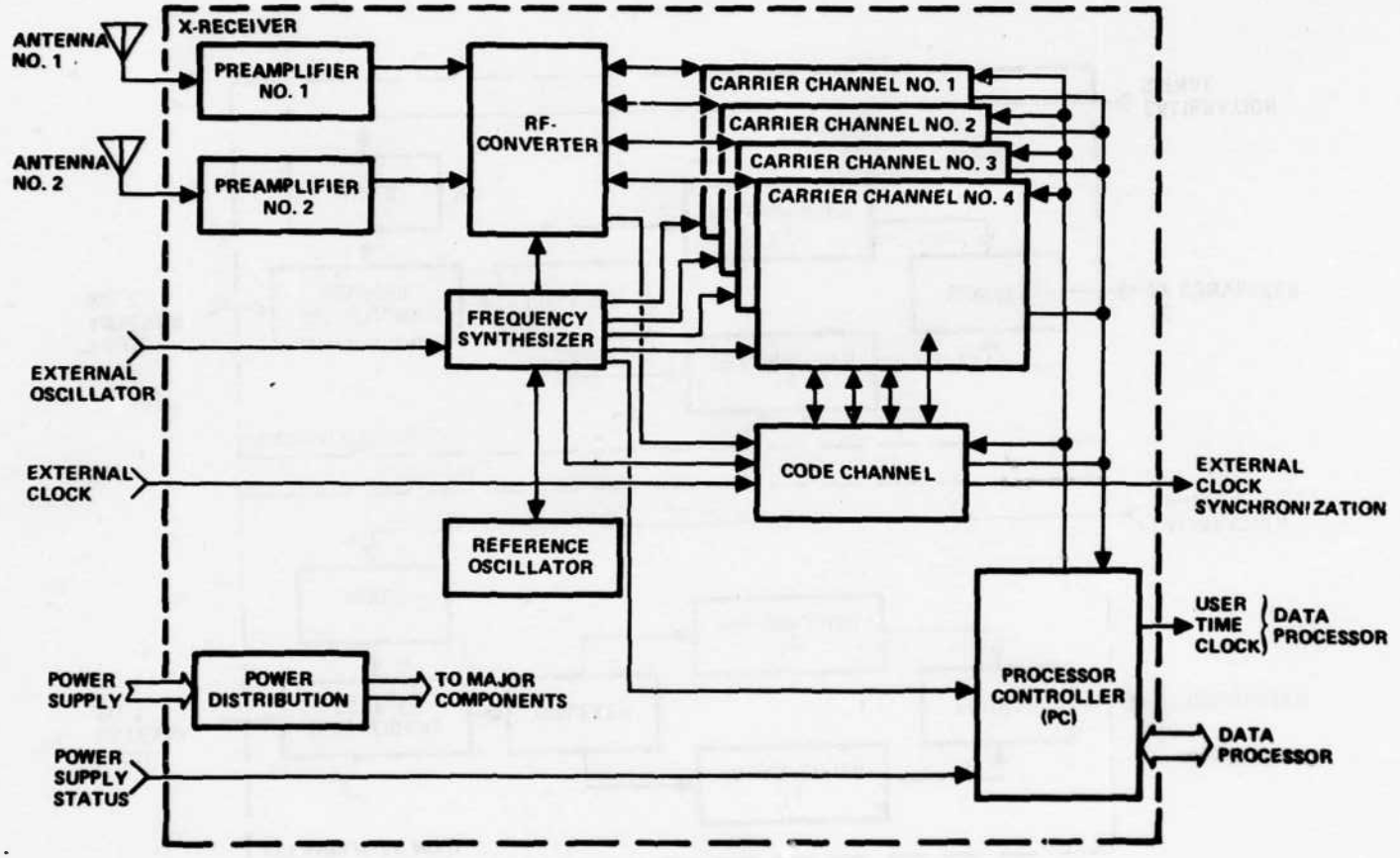



Figure 2. A Functional Block Diagram of the X-Set Receiver From Reference [3]

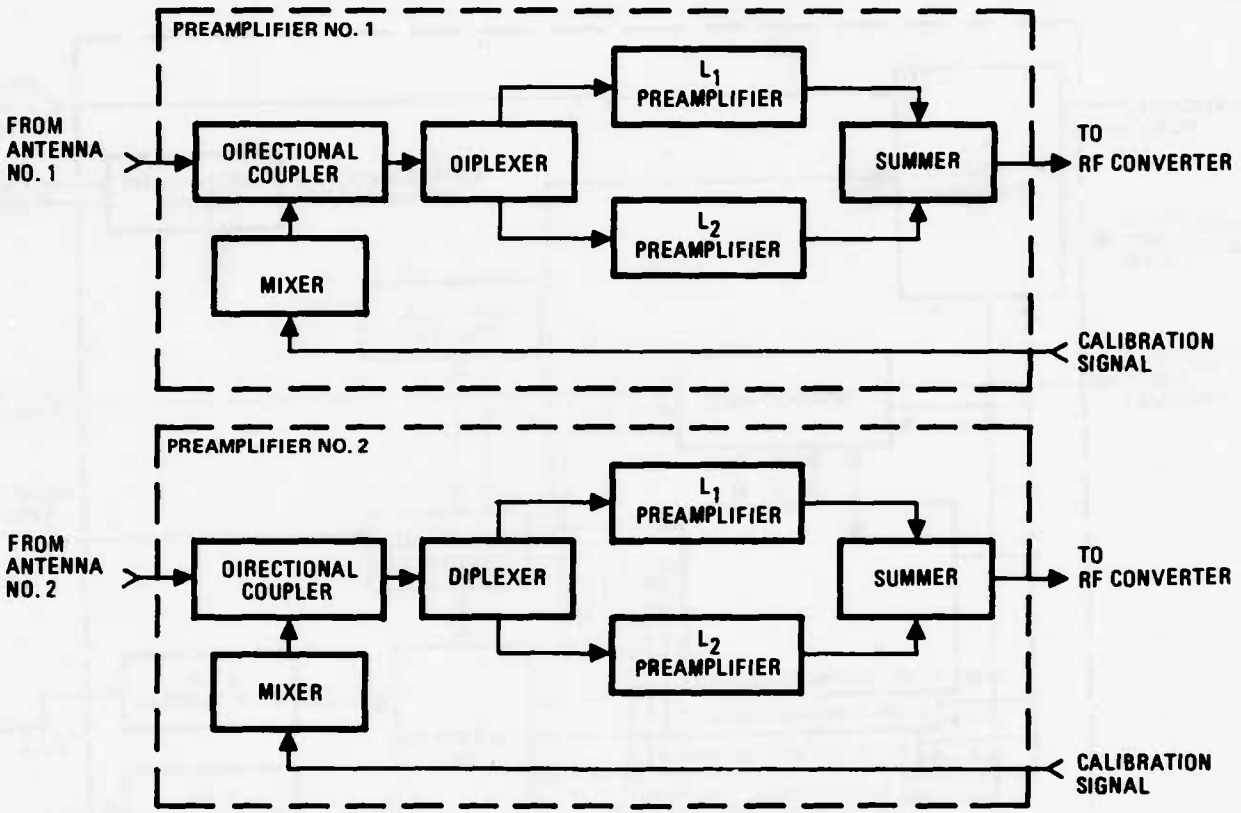



Figure 3. X-Set Preamplifier
From Reference [1]

Table 1. X-set Preamplifier Performance Specifications from References 1 and 3.

| Description | Characteristics |
|---|---|
| No. of antenna signal inputs | 1 |
| No. of calibration signal inputs | 1 |
| No. of RF signal outputs | 1 |
| Signal waveform $L_1/L_2$ | FDM |
| Nominal input/output center frequencies ($F_o$): | |
| $L_1$ | 1575.42 MHz |
| $L_2$ | 1227.60 MHz |
| $L_1$ and $L_2$ bandwidth selectivity: | |
| At -1.0 dB | ±9 MHz |
| At -3.0 dB | ±12 min. ±17 max. MHz |
| At -70.0 dB | ±70 MHz |
| Nominal input/output impedances | 50 ohm |
| Max. input/output vswr ($F_o$±8 MHz) | 1.5:1 |
| Max. noise figure | 3.5 dB |
| Reference preamplifier input: | |
| Remote located | 100 ft. max. |
| Cable loss | 4 dB max. |
| Input signal levels (including J/S): | |
| Max. | -50 dBW |
| Min. | -180 dBW |
| Dynamic range (noise level to 1-dB compression) | 130 dB |
| Burnout protection | 0 dBW min. |
| Gain at $F_o$ | 30-34 dB |
| Phase linearity (±8.0 MHz) | ±5 deg |
| Reverse isolation (min.) | 30 dB |
| Decoupling for calibration signal injection | 20 to 30 dB |
| Calibration signal input level: | |
| Max. | -120 dBW |
| Min. | -140 dBW |
| Group delay variation (over ±8.0 MHz range) | 10 nsec |
| Isolation ($L_1$ to $L_2$) | 50 dB min. |
| Calibration signal input | 274F + 34 F·PN |
| Input signal level | -34 dBW ± TBD |
| Output signal level | -37 dBW ± TBD |
| Input/output impedance | 50 ohm |
| | Note: F = 5.115 MHz |

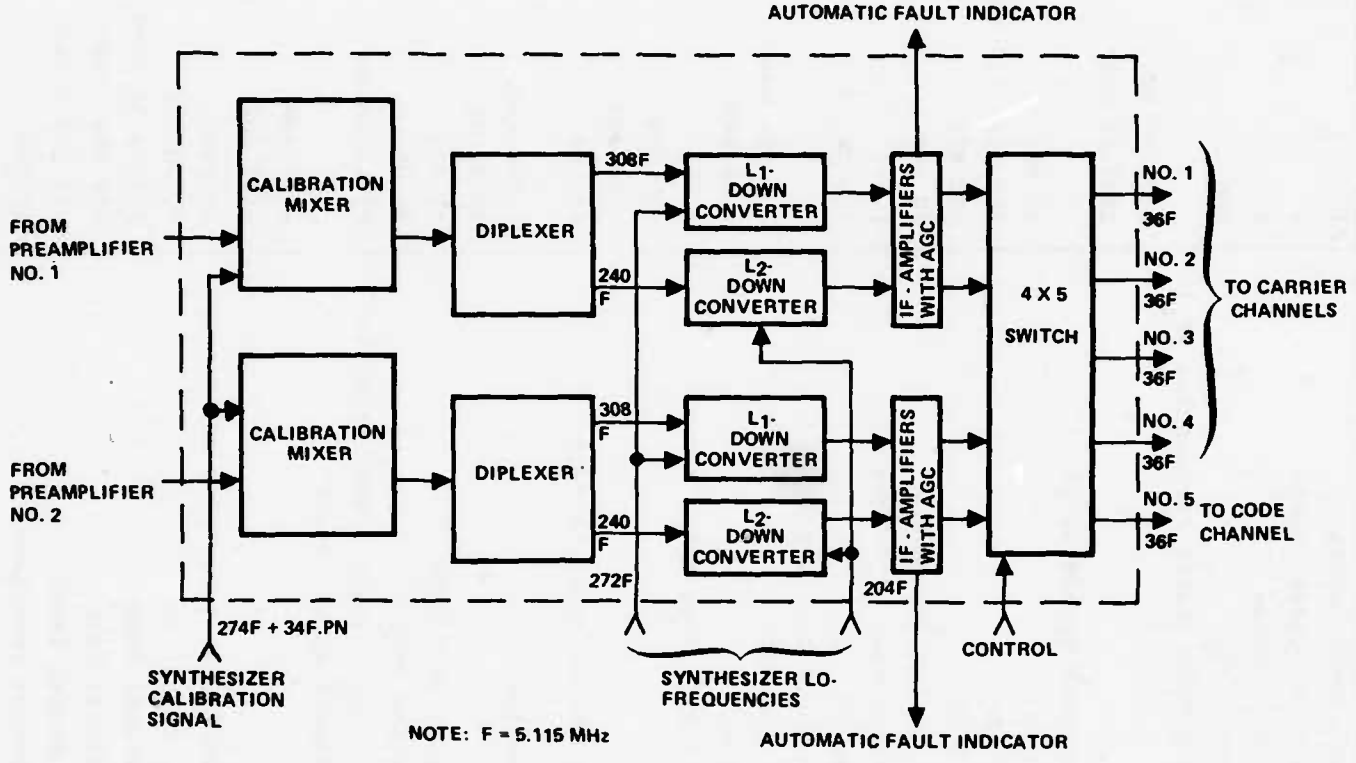



Figure 4. X-Set RF Converter
From Reference [1], Modified

noncoherent Automatic Gain Control (AGC) circuit followed by clippers which clip at an output level approximately 3 dB above the noise level. The outputs of the four IF amplifiers go to a 4X5 switch which can switch any one of the four inputs (two antennas, two frequencies each) to any one of the five outputs (four carrier channels, one code channel). The RF-converter performance characteristics are presented in Table 2.

The carrier channel as defined in reference [3] and shown in Figure 5 consists of a local reference generator/correlator, signal conditioner, carrier rate multiplier/incremental phase modulator, code rate multiplier/incremental phase modulator, code generator, and address selector/data director. The functional operation of each of these units is described in the following paragraphs.

The local reference generator/correlator heterodynes the carrier estimate (nominally 0.25F = 1278.75 kHz) from the carrier rate multiplier/incremental phase modulator to a nominal frequency of 29.25F = 149.61375 MHz. The estimated code (in this case the on-time code estimate) is superimposed upon this signal to form the local reference for this channel. The local reference generator/correlator also amplifies the signal from the RF converter in a coherent AGC (controlled by the process controller) and correlates it with the local reference for this channel. This correlation generates a second IF of nominally 6.75F = 34.52625 MHz which goes to the signal conditioner.

The signal conditioner heterodynes the output of the local reference generator/correlator to the detection frequency, nominally 0.25F = 1278.75 kHz. It then correlates this signal with quadrature signals of fixed frequency 0.25F and integrates the outputs for a period of time (T). At the end of this time interval the outputs of the integrators are sampled and reset. The samples are converted to eight-bit binary words. Depending upon the operation the receiver is performing, T is either one or four milliseconds. In general, if the receiver is in an acquisition mode, T is one millisecond, otherwise T is four milliseconds. A more detailed discussion of the local reference generator/correlator and signal conditioner is given in a subsequent section on the implementation of the Costas loop in the X-set.

The carrier Rate Multiplier/Incremental Phase Modulator (RM/IPM) is essentially a digital Voltage-Controlled Oscillator (VCO). Figure 6 is a block diagram of the carrier RM/IPM. Every 4 ms the process con-

Table 2. X-set RF Converter Performance Specifications from References 1 and 3.

| Description | Characteristics |
|---|---|
| No. of RF inputs | 2 |
| No. of LO inputs | 2 |
| No. of IF outputs | 5 |
| Nominal RF input center frequencies ($F_o$): | |
| $L_1$ | 1575.42 MHz |
| $L_2$ | 1227.60 MHz |
| Nominal IF output center frequency | 184.14 MHz |
| $L_1/L_2$-bandwidth selectivity: | |
| At -1 dB | ±9 MHz |
| At -3 dB | ±11 min., ±17 max. MHz |
| At -70 dB | ±150 MHz |
| Nominal input/output impedances | 50 ohm |
| Max. input/output VSWR | 1.5:1 |
| Max. noise figure | 23 dB |
| Input signal levels: | |
| Max. | -50 dBW |
| Min. | -150 dBW |
| Dynamic range (gain compression to 1 dB) | 100 dB |
| Pulse-clipping level (output referenced): | -40 dBW |
| Overload recovery | 100 nsec max. |
| Gain at $F_o$ | 55 dB |
| Output power level at 1 dB gain compression | -45 dBW |
| Phase linearity (±8.0 MHz) | 10 deg |
| Output IF switching time: | 2 μsec max. |
| Isolation: | |
| Between down-conversion channels | 30 dB |
| Between LO inputs | 20 dB |
| Between IF outputs | 30 dB |
| Between LO inputs and IF outputs | 30 dB |
| Calibration signal: | 274F + 34F · PN |
| Output signal level | -120 dBW ± 5 |
| Input signal level | -50 dBW ± 5 |
| Input/output impedance | 50 ohm |
| Calibration command: | |
| Signal levels | TTL<br>Note: F = 5.115 MHz |

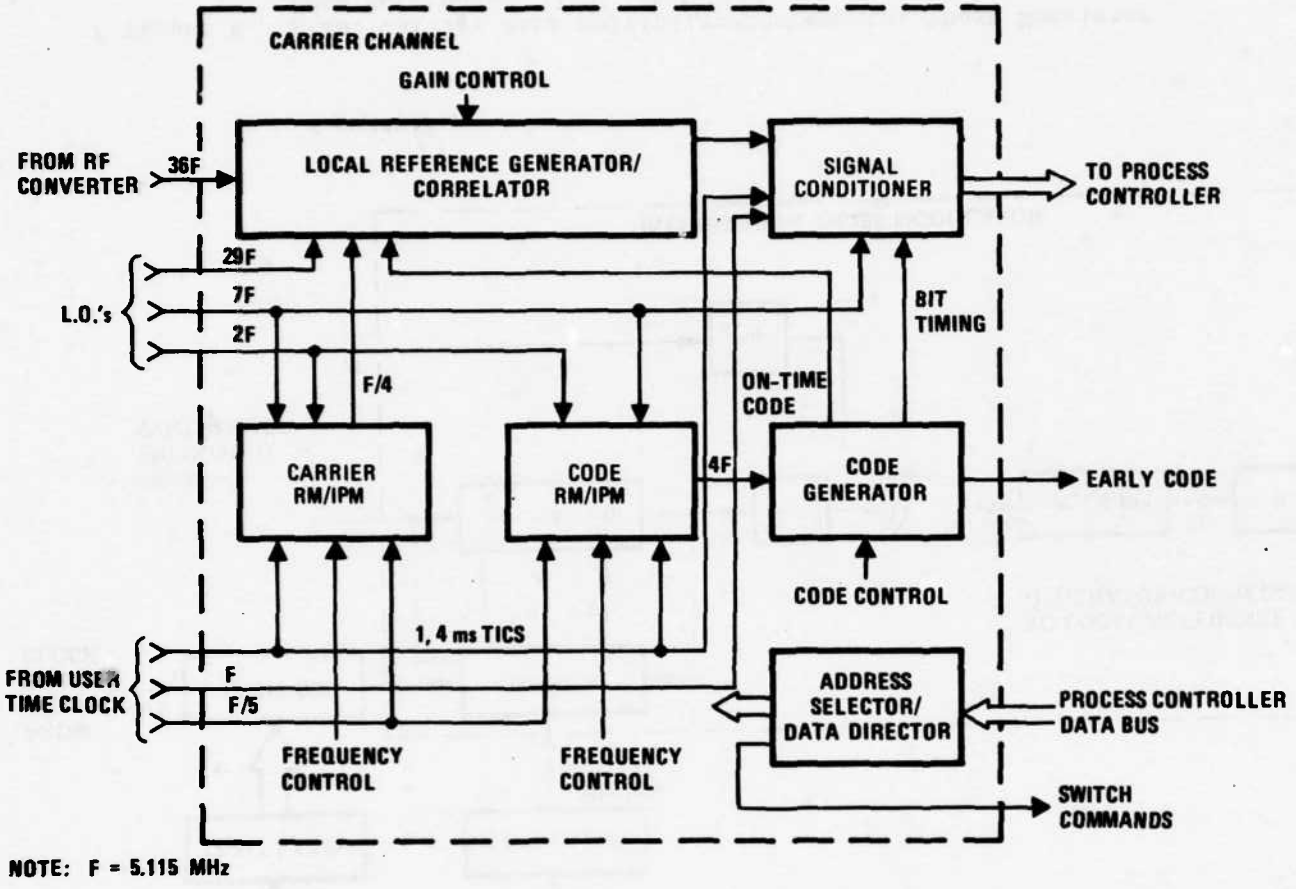



Figure 5. X-Set Carrier Channel
From Reference [1], Modified

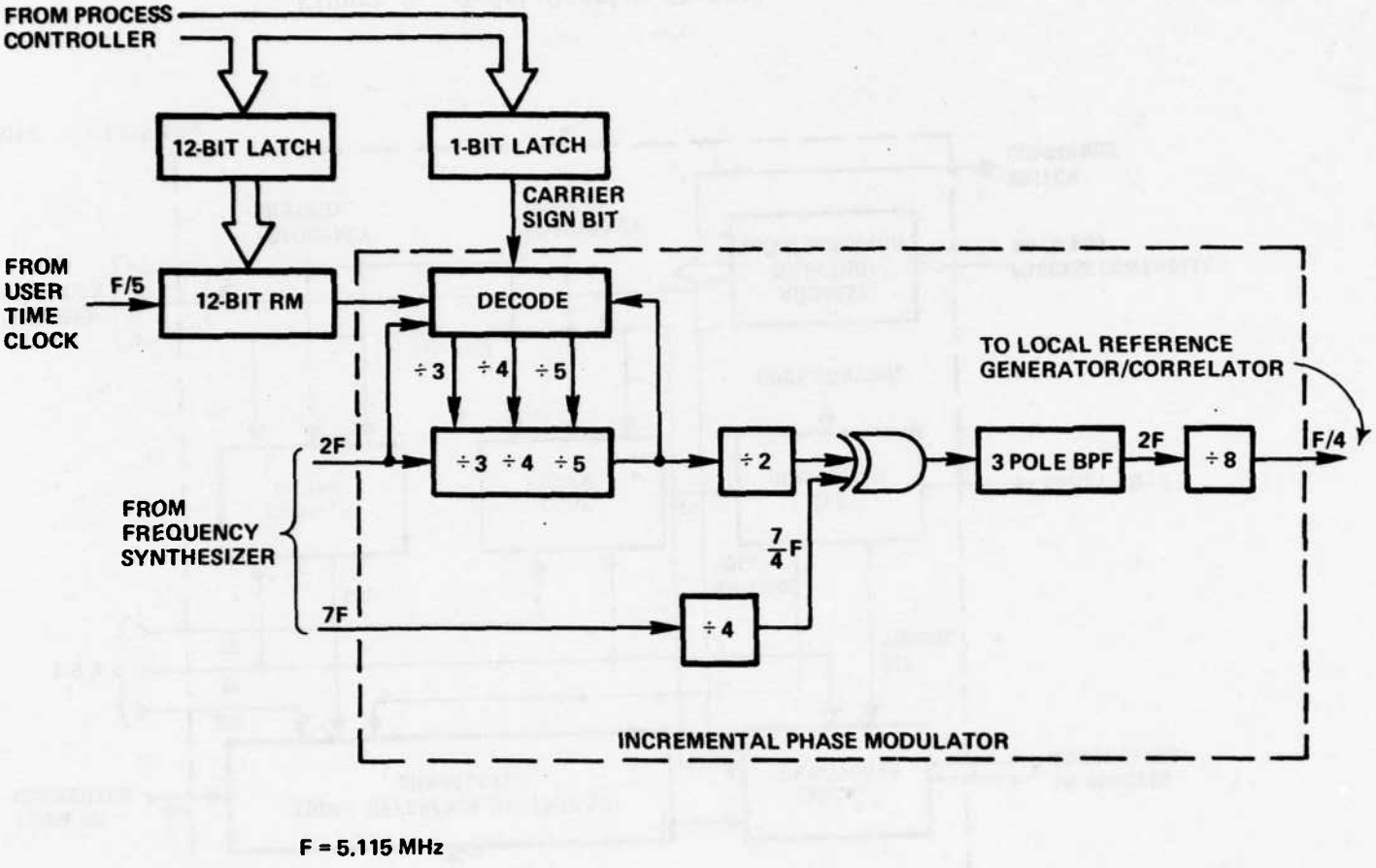



Figure 6. X-Set Carrier Rate Multiplier/Incremental Phase Modulator From References [1,3], Modified

troller supplies a twelve-bit control word, FREQ, to the RM and a one-bit control word to the IPM. The output frequency of the RM is equal to

$$(F/5)\left(\frac{FREQ}{4092}\right) \qquad (1)$$

where F = 5.115 MHz. The IPM operates in the following manner. The phase of the output signal is advanced or delayed by dividing a reference signal of frequency 2F by either three, four, or five. The divider is controlled by the output of the RM and the carrier sign bit. The output of the RM indicates whether the output phase should be changed or not and the carrier sign bit indicates in which direction the phase should change to drive the loop error to zero. If the phase is to remain the same, the divider divides by four. If not, the divider divides by either three or five depending upon whether the phase is to be advanced or delayed. Then the IPM divides the output of the variable-modulus divider by two and heterodynes the signal with the fixed frequency 1.75F = 8.95125 MHz. It selects the sum-frequency, 2F = 10.23 MHz, output of the heterodyner with a three-pole band-pass filter and divides this signal by eight to produce the phase-modulated output signal of frequency 0.25F = 1278.75 kHz. A change of one least-significant bit in FREQ causes a change of 1/64 of a cycle every 4 ms in the output of the RM/IPM.

The code RM/IPM is shown in block diagram form in Figure 7. Its operation is similar to that of the carrier RM/IPM except that only a five-bit word is used to control the RM and that the output of the IPM is generated by dividing the output of the first band-pass filter by two, heterodyning this signal with 3.5F = 17.9025 MHz, and selecting the sum-frequency, 4F = 20.46 MHz, output of the heterodyner with a two-pole band-pass filter. As with the carrier RM/IPM a change of one least-significant bit in the control word causes a change of 1/64 of a chip every 4 ms in the output of the code RM/IPM.

The code generator shown in Figure 8 generates both the C/A (Gold) and P codes. It also generates channel interrupts at either 1- or 4-ms periods and provides a bit clock. Four twelve-stage linear feedback shift registers are used to generate the P code. The outputs of the X1A and X1B registers are modulo-2 summed to form the output of the X1 register. The outputs of the X2A and X2B registers are added modulo-2 to generate the output of the X2 register. The P code is formed by modulo-2 adding the outputs of the X1 and X2 registers. Upon receiving

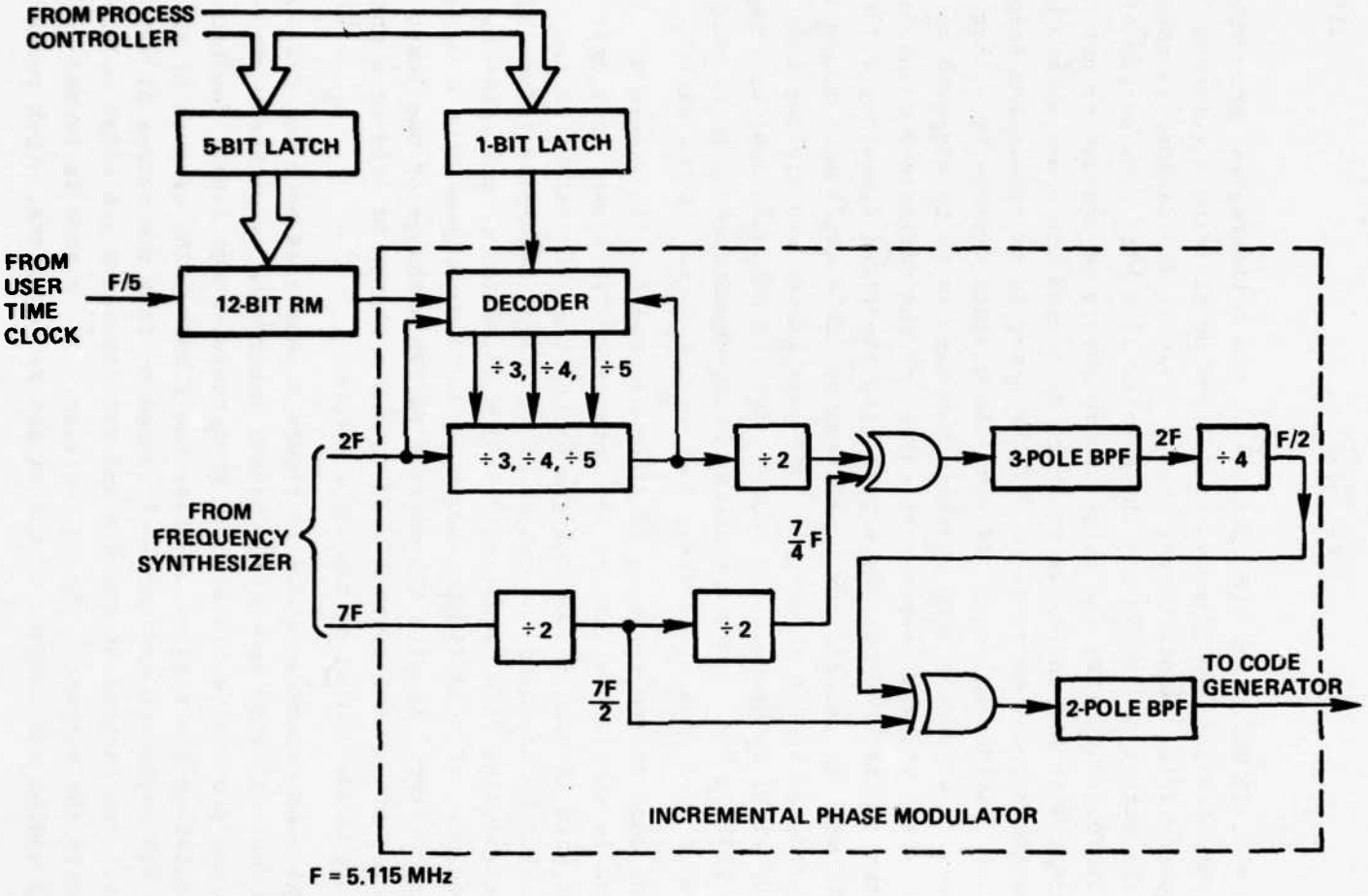



Figure 7. X-Set Code Rate Multiplier/Incremental Phase Modulator From References [1,3], Modified

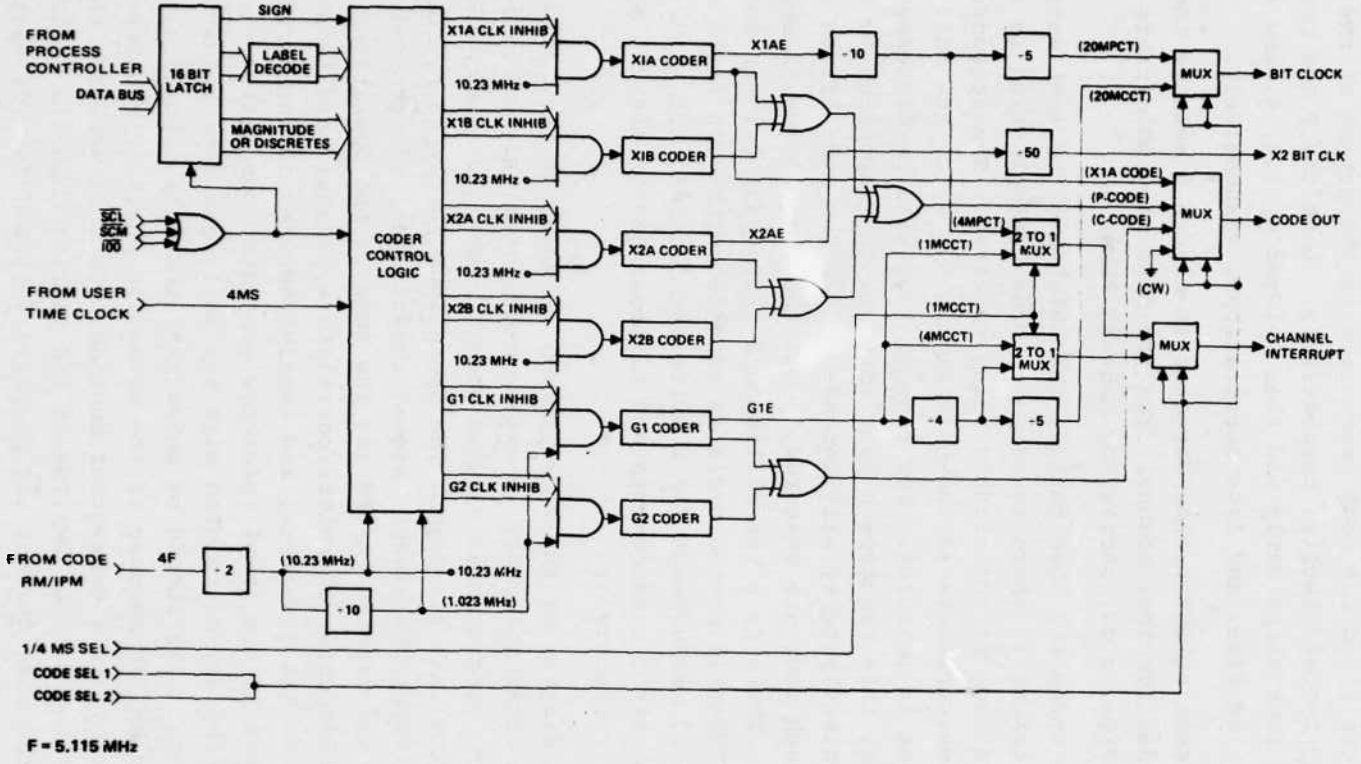


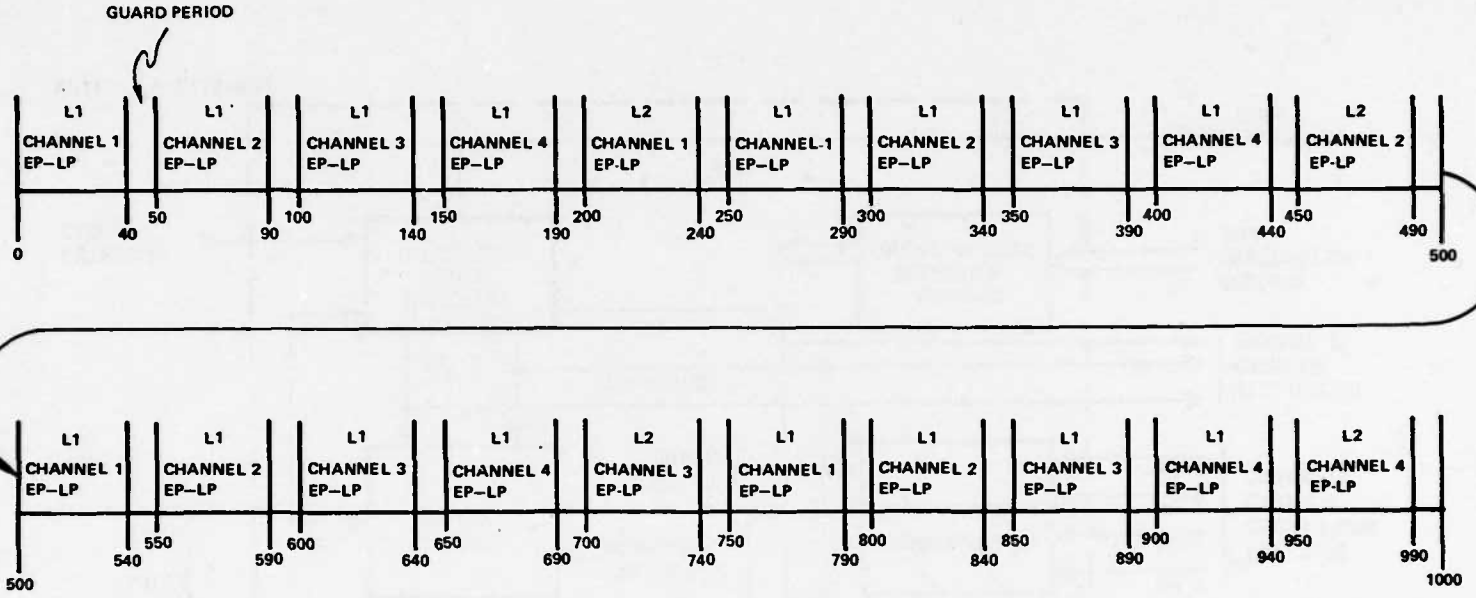

Figure 8. X-Set Code Generator
From Reference [1]

the proper commands from the process controller the code generator can set the epoch of the X1 register and slew the X2 register to any value in less than 1.62 seconds. The C/A (Gold) code is generated by modulo-2 summing the outputs of two ten-stage linear feedback shift registers. The input to the P and C/A code generators is the output of the code RM/IPM divided by two and twenty, respectively. Both the P and C/A codes are generated four chips early and then delayed by 3.5, 4, and 4.5 chips for the early, on-time, and late correlations, respectively.

The address selector/data director in Figure 5 selects the data that is intended for that channel from the data bus and directs it to the proper device, e.g., carrier or code RM/IPMs.

Whereas there are four carrier channels (one for each satellite signal being tracked), there is only one code channel which is time shared between each of the signals being received. The sequence of code channel measurements is shown in Figure 9. First the code error for channel one is measured. For reasons that will be discussed in later sections, this requires a time interval corresponding to two data bits or equivalently forty milliseconds. Then the code errors for channels two through four are measured. Next the channel-one L2 measurement is made. There is a ten-millisecond guard band between measurements. This 250-millisecond cycle is repeated with each fifth measurement being an L2 measurement for a different channel. Thus the update rates for code-error measurements and L2 measurements are 250 and 1000 milliseconds, respectively.

A block diagram of the code channel is shown in Figure 10. It consists of a local reference generator/correlator, signal conditioner, carrier RM/IPM, programmable digital delay, user time clock, and an address selector/data director. The operations performed by the local reference generator/correlator, signal conditioner, address selector/data director and carrier RM/IPM are the same as the operations performed by the local reference generators/correlators, signal conditioners, address selectors/data directors, and carrier RM/IPMs of the carrier channels except that in the local reference generator/correlator the incoming signal is alternately correlated with the early and late codes instead of the on-time code. (It should be noted that the code loop requires a separate carrier RM/IPM because of the manner in which L2 measurements are made, as described in a subsequent section. If this were not the case, the outputs of the carrier RM/IPMs on the carrier channels could simply be routed to the code channel and properly switched for correlation




EP–LP = EARLY POWER – LATE POWER

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Figure 9. Time Sharing Sequence of the X-Set Code Channel While in the Tracking Mode From Reference [3]

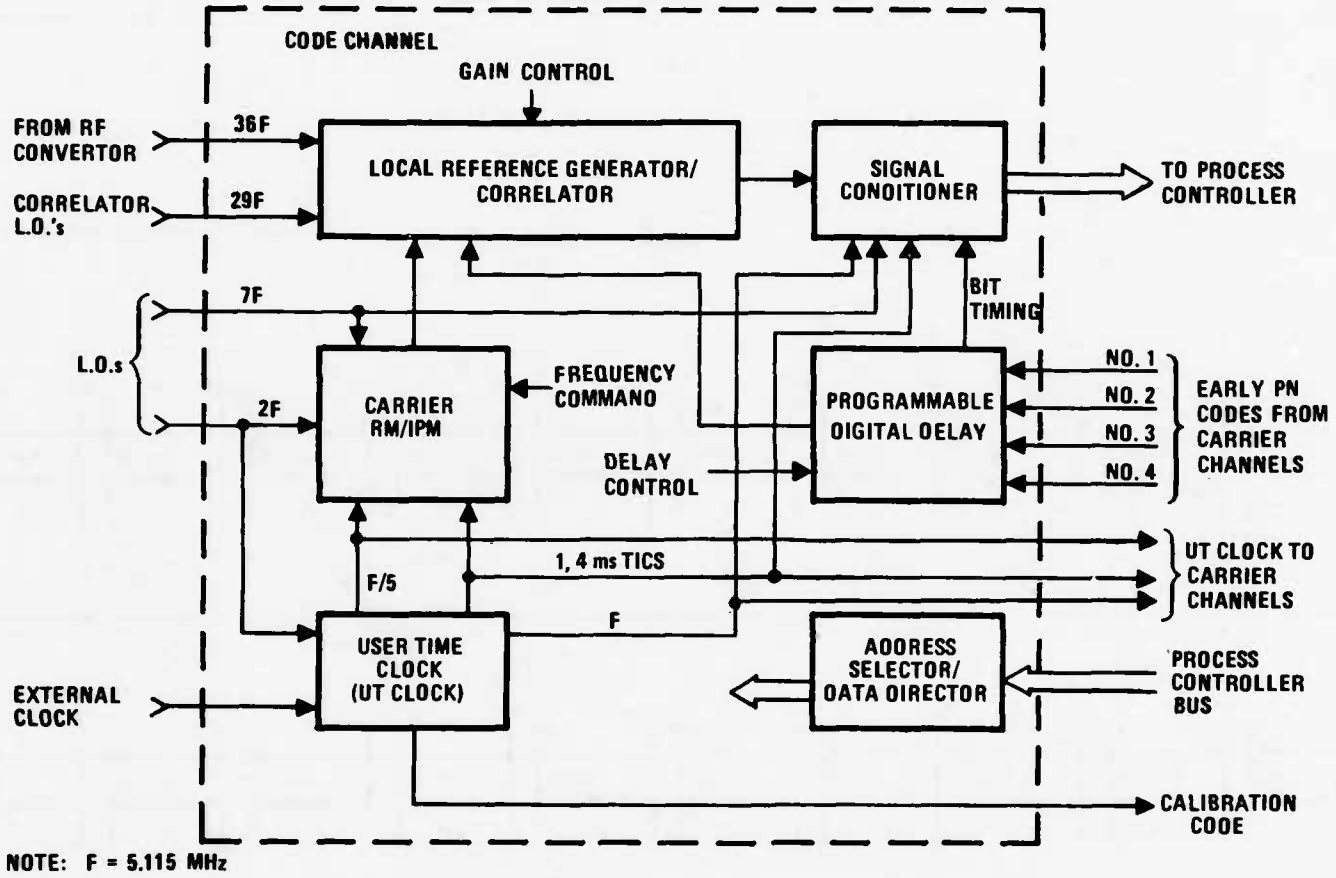



Figure 10. X-Set Code Channel
From Reference [1], Modified

with the incoming signal).* The functional operations of the user-time clock and the programmable digital delay are described in the following paragraphs.

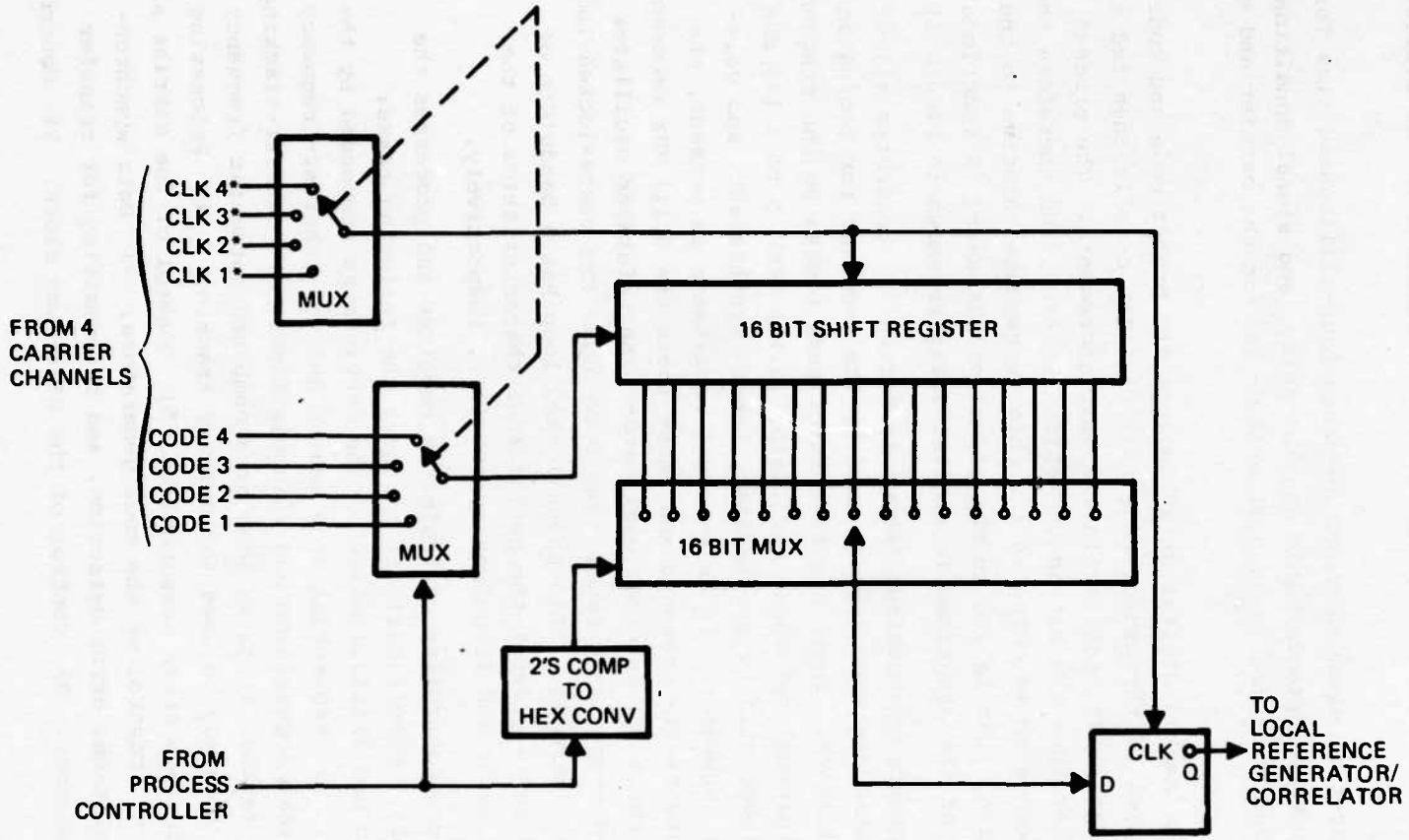
The user-time clock provides accurate four-millisecond tics for the code generators, programmable digital delay, and signal conditioners and timing signals of frequency 0.2F = 1023 Hz for the carrier and code RM/IPMs.

The programmable digital delay selects the proper code and code clock (the output of the proper code RM/IPM). The code is then fed into a sixteen-bit shift register in 1/2 chip increments. The process controller determines the bit in the shift register, and therefore the code delay from -4 to +4 chips in 1/2 chip increments relative to the on-time estimate, that is fed to the signal conditioner. A functional block diagram of the programmable digital delay is shown in Figure 11.

The frequency synthesizer (shown in Figure 12) generates all of the stable continuous wave signals used by the receiver for timing and as local oscillators. There are five functional blocks to the frequency synthesizer, internal reference oscillator (5.115 MHz), 5 to 5.115 MHz phase-locked loop, utility synthesizer, L-band synthesizer, and calibration signal generator. If an external oscillator is present, the synthesizer detects its presence and phase locks the 5.115 MHz reference oscillator to the 5 MHz external oscillator. The reference oscillator can be adjusted over a 4 Hz range. The 5 to 5.115 MHz phase-locked loop is depicted in Figure 13. This phase-locked loop has a bandwidth of 1 Hz. Tables 3 and 4 present the performance characteristics of the reference oscillator and frequency synthesizer, respectively.

The process controller controls the receiver and processes the incoming signals. Specifically it performs the following tasks: 1) Calibration and initialization of the receiver as commanded by the data processor. 2) Sequential code search and non-coherent-frequency pull-in for signal acquisition and reacquisition. 3) Carrier-tracking loop selection (either a Costas loop or a combined automatic frequency control/Costas loop may be used for carrier tracking). 4) Processing of carrier and code loop error measurements. 5) Control of the carrier and code RM/IPMs. 6) Control of the code generators. 7) Data synchronization, demodulation, error detection, and reformatting for transfer to the data processor. 8) Control of the user-time clock. 9) Control

*The number of leads running between modules may also be a consideration.




*NOTE CLKS 1-4 ARE THE OUTPUTS OF THE CODE RM/IPMs ON CARRIER CHANNELS 1-4, RESPECTIVELY.

Figure 11. X-Set Code Channel Programmable Digital Delay From Reference [1]

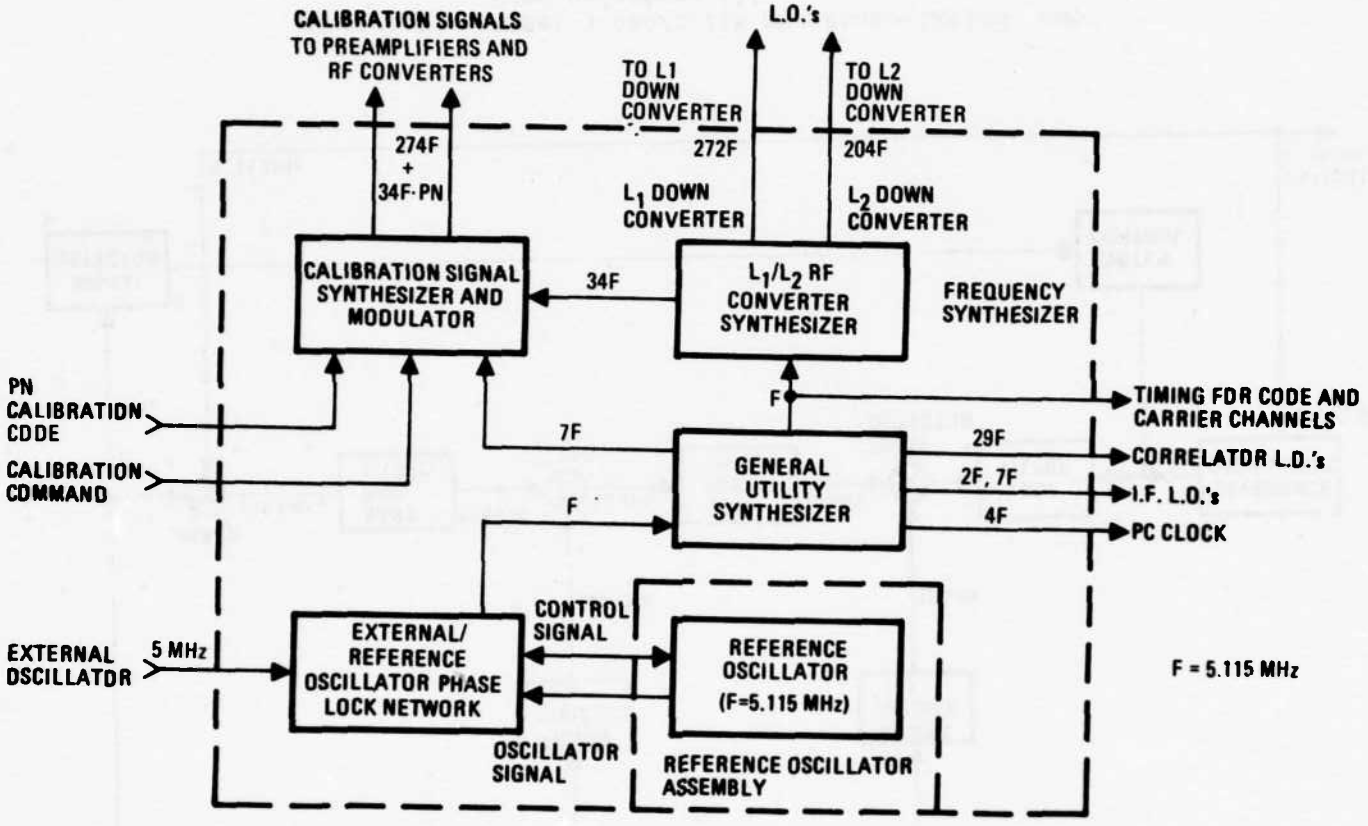



Figure 12. X-Set Frequency Synthesizer/Reference Oscillator
From Reference [1], Modified

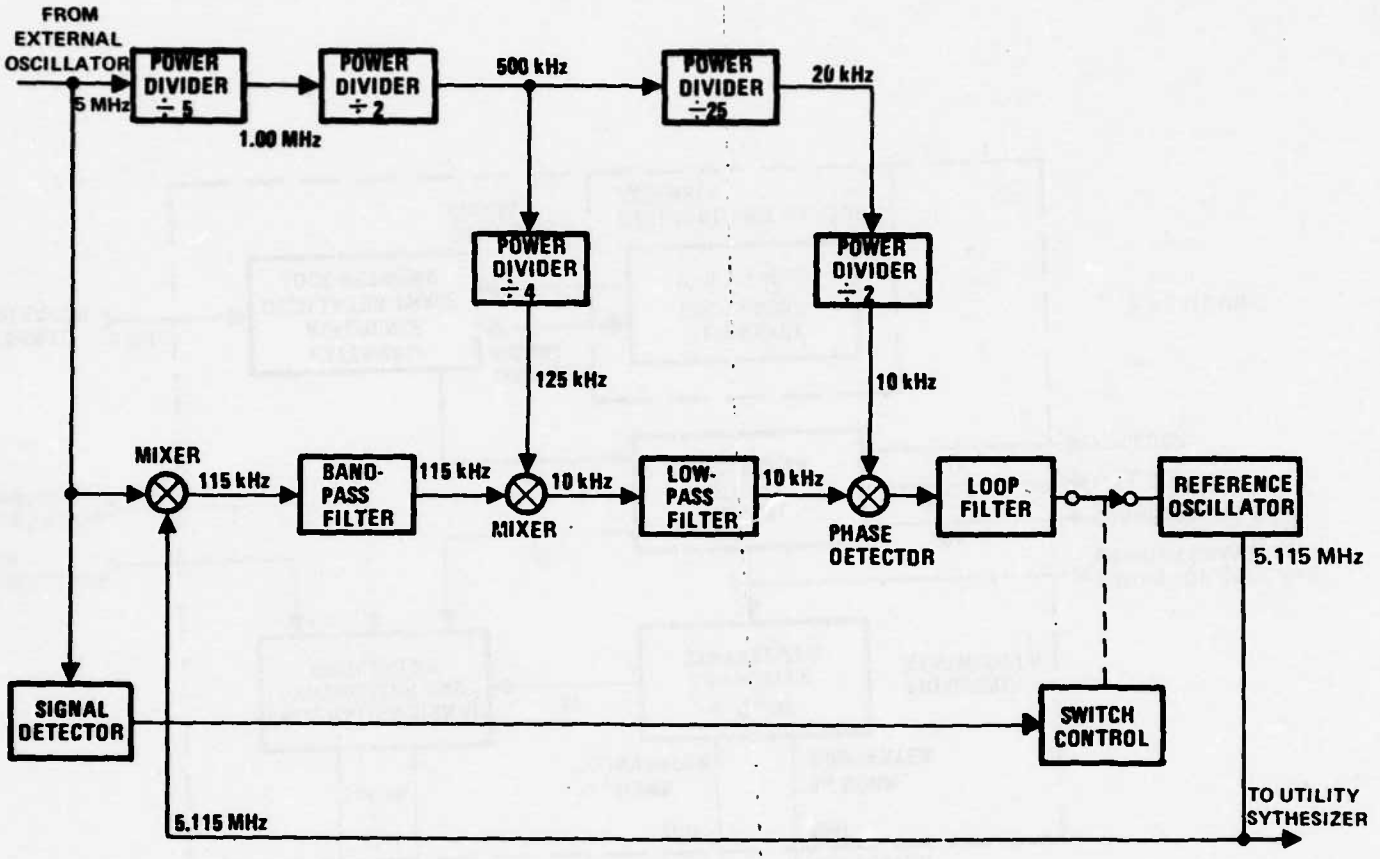



Figure 13. X-Set 5.000/5.115 MHz Phase-Locked Loop
From Reference [1]

Table 3. X-set Reference Oscillator Performance Specifications from References 1 and 3.

| Description | Characteristics |
|---|---|
| Nominal output frequency | 5.115 MHz |
| Frequency adjust range: | |
| Coarse | ±10 Hz min. |
| Fine | ±1 Hz min. |
| Output level (rms) | 0.5 V min. |
| Output load | 50 ohm (nominal) |
| Temperature range: | |
| Operation | -20 to +70°C |
| Storage | -65 to +125°C |
| $\frac{\Delta F}{F}$ Stability: | |
| Total frequency deviation over entire temperature range | $<1 \times 10^{-9}$ |
| Short term | $<1 \times 10^{-10}$/sec |
| Aging rate | $<1 \times 10^{-9}$/24 hr |
| Voltage | $<\pm 1 \times 10^{-9}$/±5 percent |
| Loading | $<\pm 1 \times 10^{-9}$/10 percent |
| Vibration | $<2 \times 10^{-9}$/g |
| Shock | $<2 \times 10^{-9}$/g |
| Acceleration | $<3 \times 10^{-9}$/g |
| Stabilization: | |
| From temperature: | -20°C to +70°C |
| 5 Minutes | $<1 \times 10^{-7}$ |
| 30 Minutes | $<2 \times 10^{-9}$ |
| Frequency pulling range | 0.4 ppm |

Table 4. X-set Frequency Synthesizer Performance Specifications from References 1 and 3.

| Description | Characteristics |
|---|---|
| Receiver reference oscillator frequency (F) | 5.115 MHz |
| Synthesized frequencies | 2F, 4F, 7F<br>17F, 21F, 29F, 34F,<br>204F, 272F, 274F |
| Power level for synthesized frequencies | -23 ± 3 dBW |
| Phase-noise contribution of synthesizer: | |
| LO frequencies (rms) | 2 deg |
| Timing signals | 2 deg |
| Calibration signals (rms) | 10 deg |
| Spurious level: | |
| LO outputs | -50 dB |
| Timing signals | -40 dB |
| Calibration signal | -30 dB |
| External input reference oscillator frequency: | |
| Frequency | 5.0 MHz |
| Signal level (rms) | 1.0 V |
| Nominal input/output impedances | 50 ohm |
| Max. VSWR | 2:1 max. |
| Isolation: | |
| Between LO outputs | 50 dB |
| Between LO and calibration signal outputs | 50 dB |
| Between all outputs and reference oscillator input | 50 dB |
| Between all outputs and code signal input | 40 dB |
| Calibration signal | 274F + 34F · PN<br>Note: F = 5.115 MHz |

of the coherent AGC circuitry. 10) Signal quality monitoring. 11) Measurement of the pseudo-range, delta-range, and L1-L2 code signals for each satellite signal being tracked.

With the exception of the signal monitoring functions, the operations of the process controller are described in the succeeding sections.

## Section 4. Costas Loop Implementation

Under normal tracking conditions, i.e., good signal-to-noise ratios, the X-set receiver employs a Costas loop for carrier tracking*. A block diagram depicting the implementation of the Costas loop in the X-set is shown in Figure 14. The input from the RF converter at the first IF of 36F (F = 5.115 MHz) is

$$D(t-\tau)C(t-\tau)\sin(36\omega t+\theta) \qquad (2)$$

Where $D(t-\tau)$ is the received data modulation, $C(t-\tau)$ is the received pseudo-random code, $\tau$ is the propagation delay, $\omega = 2\pi F$, and $\theta$ is the phase of the received signal. (The phase $\theta$ is time varying and includes any Doppler shift in the received signal due to satellite and vehicle motion). This signal is amplified in a coherent Automatic Gain Control (AGC) circuit, where the gain is controlled by the process controller and is dependent upon the magnitude of the inphase signal component.

The output of the AGC circuit is multiplied by the feedback waveform

$$C(t-\hat{\tau})\cos(29.25\omega t+\hat{\theta}) \qquad (3)$$

Where $\hat{\tau}$ is the code-tracking loop estimate of the delay of the incoming pseudo-random code, and $\hat{\theta}$ is the estimate of the received carrier phase. Considering only difference-frequency terms, the signal at point A is at a second IF of 6.75F and is

$$D(t-\tau)C(t-\tau)C(t-\hat{\tau})\sin(6.75\omega t+\theta-\hat{\theta}) \qquad (4)$$

So far all of the operations described are performed in the local reference generator/correlator section. Now the operations performed in the signal conditioner section will be discussed. The signal at point A is heterodyned to F/4 and correlated with $\sin\left(\frac{\omega}{4}t\right)$ and $\cos\left(\frac{\omega}{4}t\right)$ to produce the signals

$$D(t-\tau)C(t-\tau)C(t-\hat{\tau})\cos(\theta-\hat{\theta}) \qquad (5)$$

*Just prior to the printing of this report, except for those receivers employed at the monitor stations, the combined AFC/Costas loop originally intended for use in the HOBYT mode (see Sections 5 and 7) was being considered for carrier tracking in normal tracking conditions. As of yet, a decision has not been made.

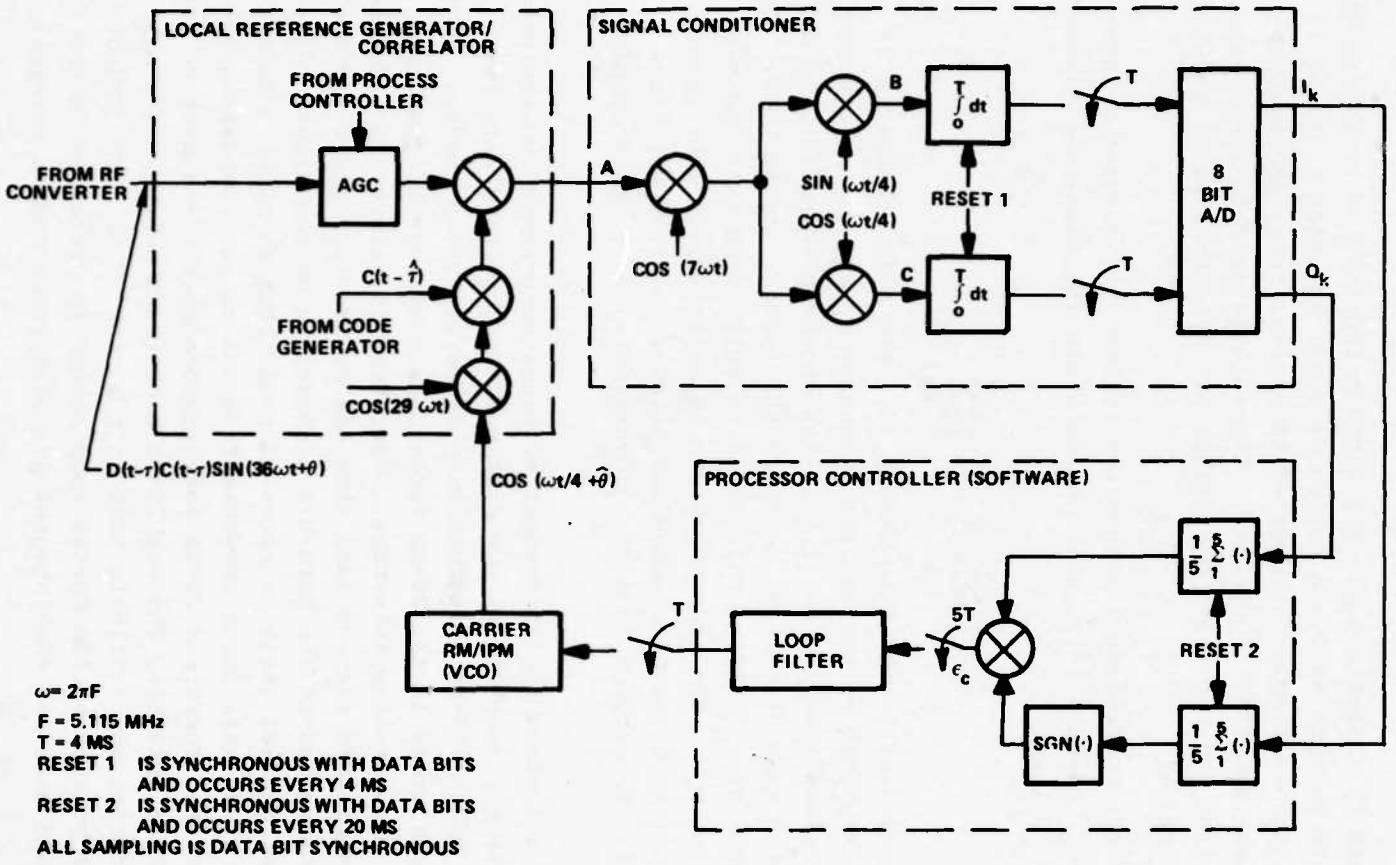



Figure 14. X-Set Costas Loop Implementation From References [1-8]

and

$$D(t-\tau)C(t-\tau)C(t-\hat{\tau})\sin(\theta-\hat{\theta}) \qquad (6)$$

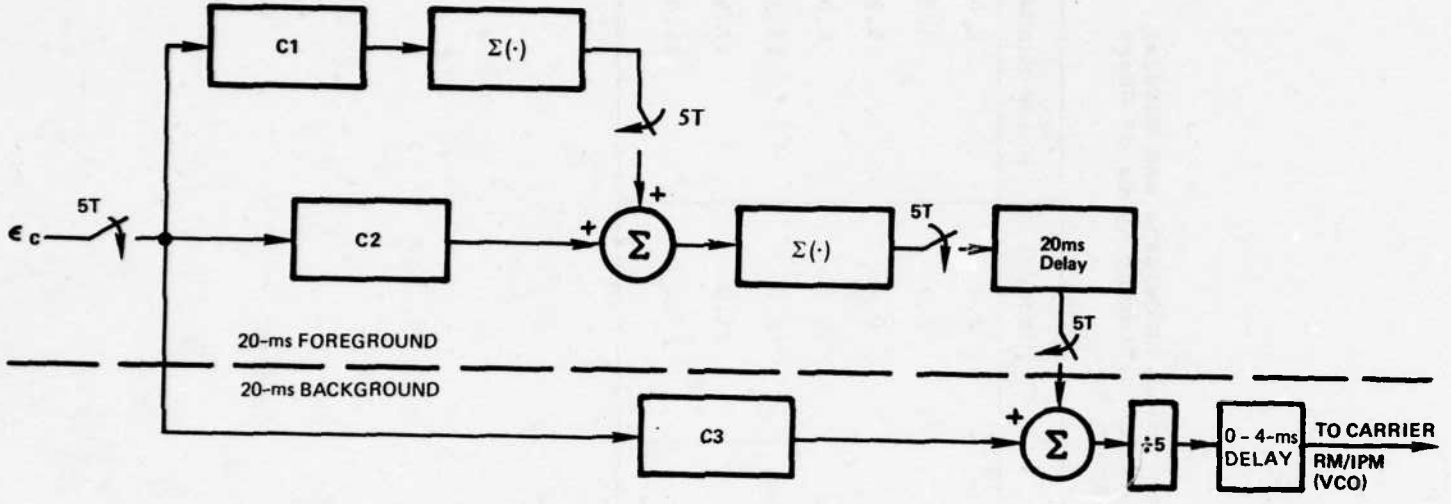
at points B and C, respectively. The signals represented by Equations (5) and (6) are integrated for a period of 4 ms, at which time the integrator outputs are sampled, converted to digital form, and held by an 8-bit analog-to-digital converter. The integrators are then reset. Both the sampling and the reset operations are synchronized to the incoming data bits.

The process controller averages the inphase and quadrature samples, $I_k$ and $Q_k$, respectively, over one data bit and forms the Costas loop error as follows.

$$\varepsilon_c = \left[\frac{1}{5}\sum_{k=1}^{5} Q_k\right]\left[\text{sgn}\left(\frac{1}{5}\sum_{k=1}^{5} I_k\right)\right] \qquad (7)$$

The loop filter is shown in Figure 15. The noise bandwidth of the loop is determined by the natural frequency $\omega_n$ and may assume seven discrete values from 2.1 to 21 Hz. The choice of bandwidth is dependent upon the type of vehicle in which the X-set is to be used. The allowable values of $\omega_n$ and the situations in which each is to be used are shown in Table 5. The loop bandwidth is selected via four binary bits, therefore there are nine bandwidth-selection states which are not being used. No attempt is made to dynamically vary the loop bandwidth.

To help alleviate the throughput problems experienced by the process controller the loop filter computations are separated into two computational modes; 20-ms foreground and 20-ms background modes. Those computations performed in the 20-ms foreground mode must be completed by the next 4-ms user-time interrupt. User time is asynchronous to the inphase and quadrature samples (and thus the Costas-loop error samples) which are synchronized to the data-bit transitions of the signal being tracked by that channel (this is referred to as channel time). Thus a user time interrupt will occur anywhere from 0-4 ms after updating the Costas loop error. Therefore 20-ms foreground computations must be performed as fast as possible, whereas 20-ms background computations may be performed during any available time in the next 20 ms. The proportional (phase) portion of the Costas loop filter is performed in the 20-ms foreground mode and the integral (velocity) and double integral




T = 4 MS
ALL SAMPLING IS DATA BIT SYNCHRONOUS
NOISE BANDWIDTH OF LOOP IS DISCRETE
WITH VALUES FROM 2.1 – 21 Hz.

Figure 15. Costas Loop Filter
From References [1,5,6-8]

Table 5. Costas Loop Noise Bandwidths and Natural Frequencies for Different Types of Users from Reference 3.

| X-Set User | $\omega_n$ (rad/s) | Noise Bandwidth (Hz) |
|---|---|---|
| Calibration mode (all Users) | 2.4 | 2.0 |
| Monitor Stations | 4.0 | 3.3 |
| Trucks | 6.4 | 5.3 |
| Large Ships | 9.6 | 8.0 |
| Cargo Aircraft and Small Ships | 16.0 | 13.3 |
| Helicopters | 21.0 | 17.5 |
| Fighter Aircraft | 25.6 | 21.3 |

(acceleration) portions of the Costas loop filter are performed in the 20-ms background mode. The delay between the 20-ms foreground and the 20-ms background computations is constrained to be 20 ms. The output of the loop filter is divided by five and sent to the carrier Rate Multiplier/Incremental Phase Modulator (RM/IPM) at a 250 Hz rate when the next user-time interrupt occurs. The RM/IPM is essentially a digital Voltage-Controlled Oscillator (VCO) with a resolution of 1/64 of a cycle. The output of the carrier RM/IPM is modulated by the on-time code estimate from the code generator and a sinusoidal of frequency 29F from the frequency synthesizer to generate the feedback signal.

Costas lock (or lack thereof) is determined by low-pass filtering the difference between the absolute value of the inphase component $|I_k|$ and the absolute value of the quadrature component $|Q_k|$. The corner frequency is about 10 Hz when the filter indicates out-of-lock and about 1 Hz when the filter indicates lock.

## Section 5. Automatic Frequency Control/Costas Loop Implementation

In situations in which Costas lock is not possible (e.g., under high jammer-to-signal conditions or during initial acquisition), the X-set receiver must estimate the carrier frequency as well as possible so that the carrier loop can provide accurate velocity aiding information to the code loop. For these purposes Automatic Frequency Control (AFC)/Costas loops are used. Two types of AFC/Costas loops are used. For acquisition, a first-order AFC and a second-order Costas loop are used. In the Hold-On-By-Your-Teeth (HOBYT) mode, which is explained in a subsequent section, a second-order AFC and a third-order Costas loop are used*.

The operation of the hardware portions (local reference generator/correlator and signal conditioner) of the AFC/Costas loop is the same as the operation of the hardware portions of the Costas loop that was previously discussed. In fact, the same hardware is used. The differences in the two tracking modes is in the process controller (i.e., software). This is true for both types of AFC/Costas loops. The AFC/Costas loop employed in the HOBYT mode will be described first. It is shown in Figure 16. The Costas portion of the error term $\varepsilon_c$ is generated in the same manner as before. The AFC error term $\varepsilon_f$ is developed by taking the average of the cross products of the current sample, ($I_k$, $Q_k$), with the preceeding sample, ($I_{k-1}$, $Q_{k-1}$), i.e.,

$$\varepsilon_f = \frac{1}{4}\sum_{k=2}^{5}[I_{k-1}Q_k - I_kQ_{k-1}] \qquad (8)$$

Note that the cross product between samples taken when data bit transitions occur are not used in forming the frequency error, $\varepsilon_f$.

At the end of each data bit the error terms, $\varepsilon_c$ and $\varepsilon_f$, go to the loop filter, which is shown in Figure 17. The Costas noise bandwidth is the same as the noise bandwidth chosen in the Costas mode and the AFC noise bandwidth is in the range from 0.1 to 4 Hz. The output of the filter determines the correct value to be sent to the carrier RM/IPM (VCO) at the next user-time interrupt. The generation of the feedback signal is the same as in the Costas mode.

The dot product of successive 4-ms inphase and quadrature samples is low-pass filtered and compared with a threshold to determine

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*See footnote on page 32.

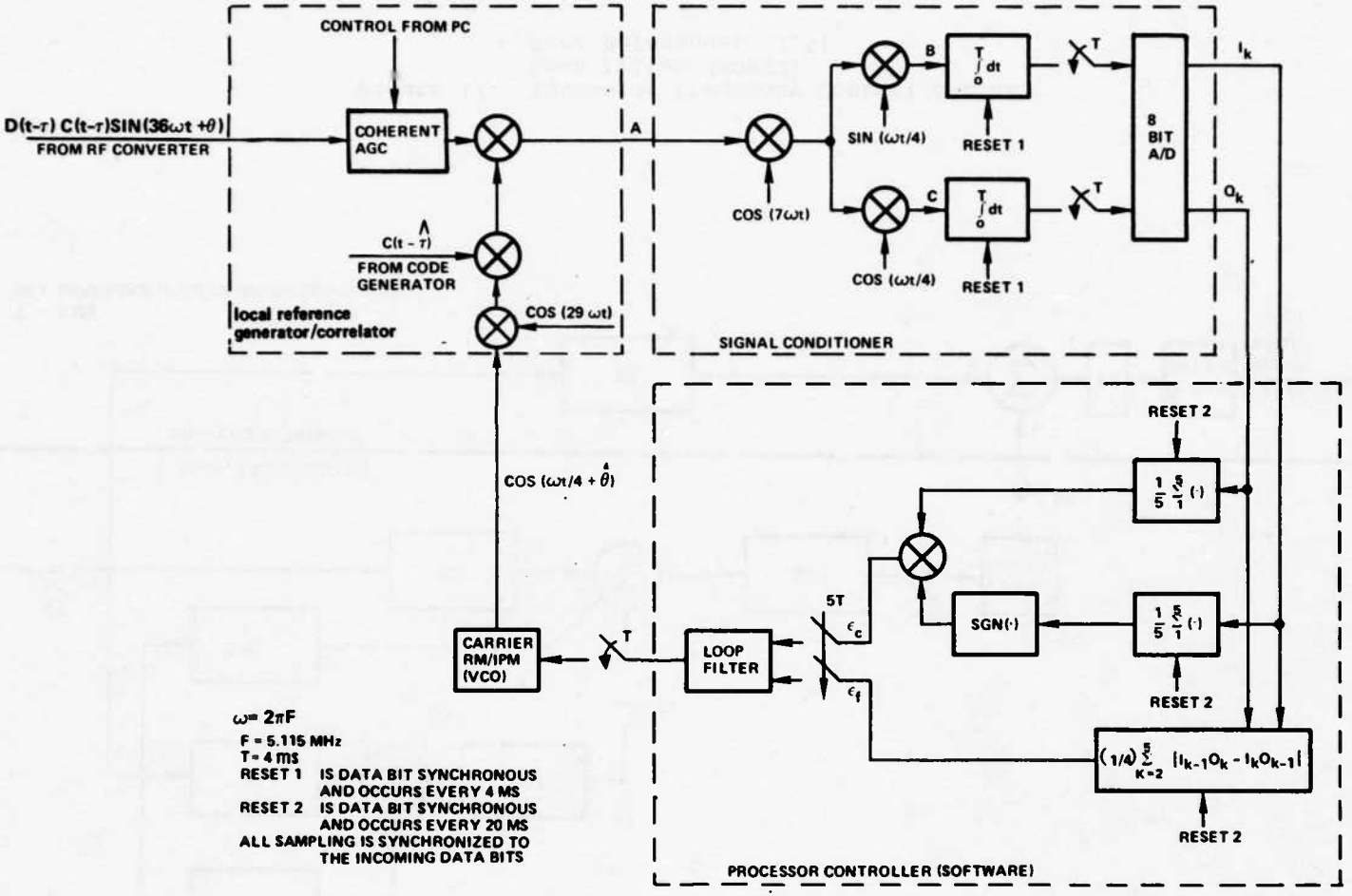


Figure 16. X-Set Automatic Frequency Control/Costas Loop Implementation (HOBYT) From References [1-5]

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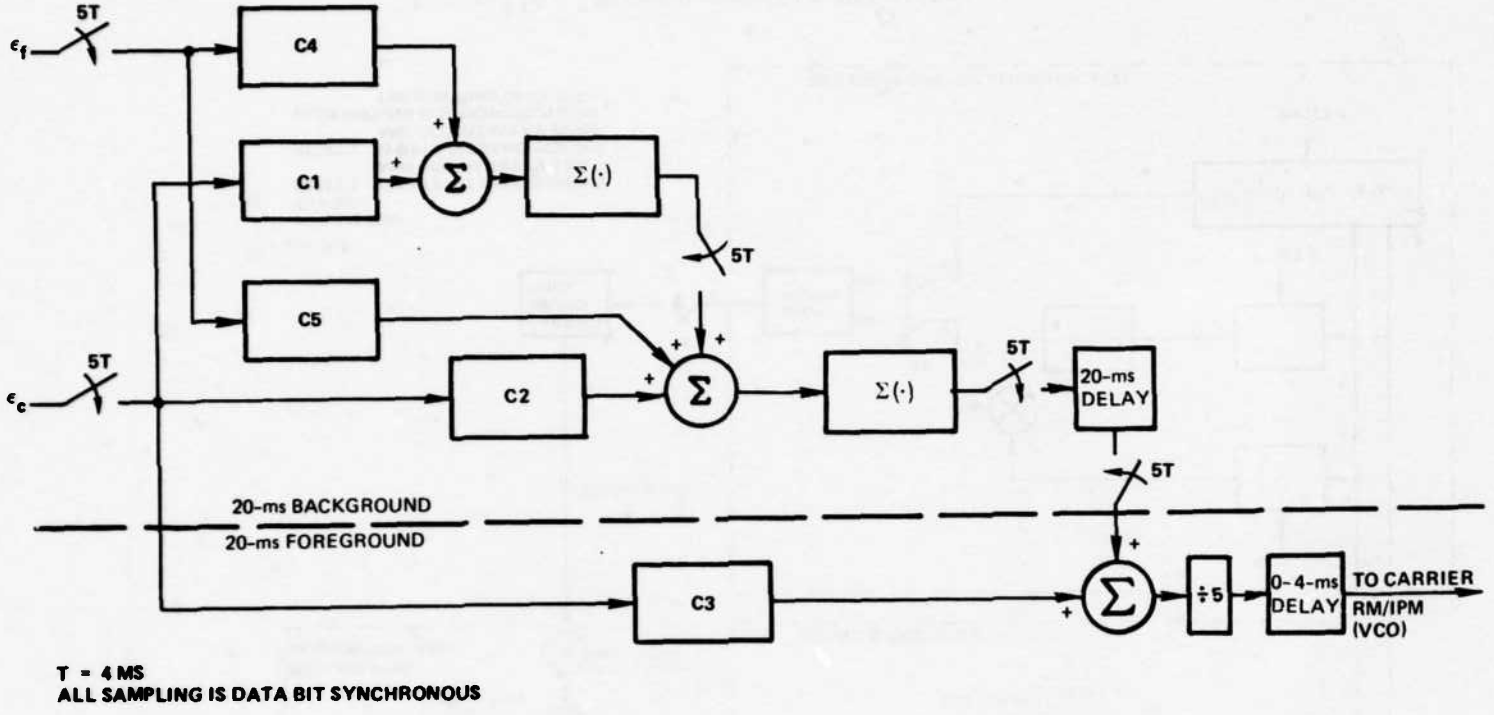


Figure 17. Automatic Frequency Control/Costas Loop Filter (HOBYT) From References [1,5]

AFC lock (or the lack thereof). The corner frequency of the low-pass filter is about 10 Hz when the filter indicates out-of-lock and about 1 Hz when the filter indicates lock.

The AFC/Costas loop employed for acquisition is shown in Figure 18. The Costas error, $\varepsilon_c$ term is formed in the following manner

$$\varepsilon_c = \frac{1}{4}\sum_{k=1}^{4} Q_k \text{sgn}(I_k) \tag{9}$$

where $I_k$ and $Q_k$ are the 1-ms inphase and quadrature samples, respectively. The AFC error term $\varepsilon_f$ is formed by taking the average of the cross produces of the current sample, $(I_k, Q_k)$, with the preceeding sample $(I_{k-1}, Q_{k-1})$, i.e.,

$$\varepsilon_f = \frac{1}{200}\sum_{k=1}^{200} [I_{k-1}Q_k - I_kQ_{k-1}] \tag{10}$$

The AFC error term is sampled by the loop filter every 200 ms whereas the Costas error term is sampled every 4 ms. The loop filter is shown in Figure 19. As previously stated, in this mode the AFC is first order and the Costas loop is second order. The output of the filter goes to the carrier RM/IPM at the user-time interrupts every 4 ms.

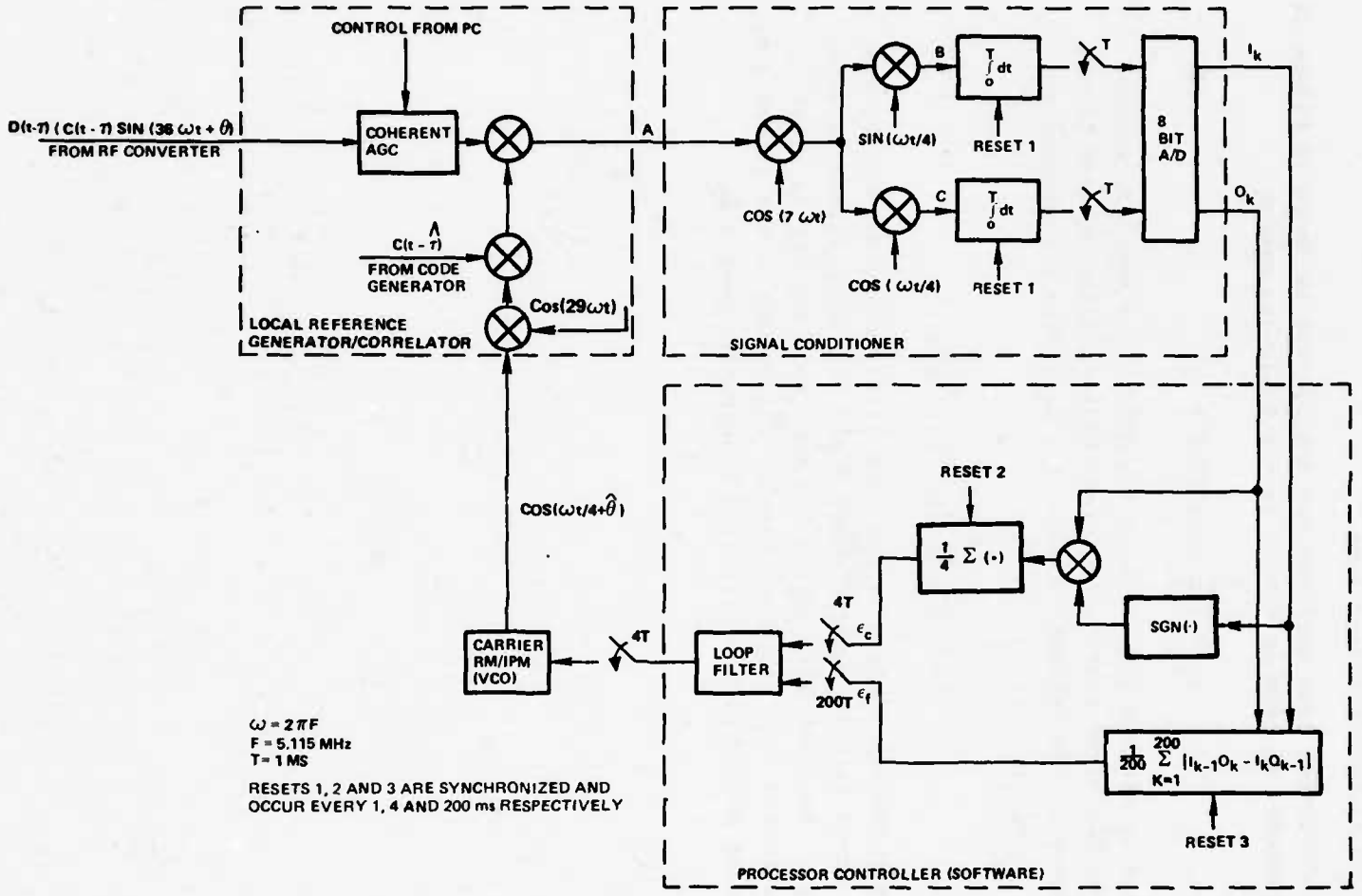


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Figure 18. X-Set Automatic Frequency Control/Costas Loop Implementation (Acquisition) From References [1,5,6-8]

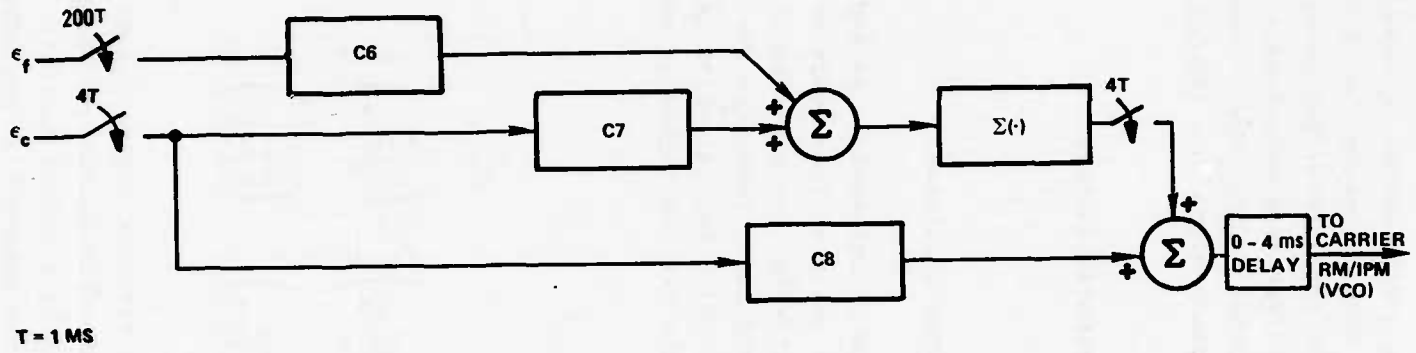


Figure 19. Automatic Frequency Control/Costas Loop Filter (Acquisition) From References [6-8]

## Section 6. Noncoherent Delay-Locked Loop Implementation

The X-set receiver employs a first-order Noncoherent Delay-Locked Loop (NDLL) for code tracking. The implementation of the NDLL in the X-set is shown in Figure 20. The local reference generator/correlator and signal conditioner operate in the same manner as the local reference generator/correlator and signal conditioner in the Costas and AFC/Costas loops. However, the feedback signal for the NDLL is alternately switched between

$$C(t-\hat{\tau}+\Delta)\cos(29.25\omega t+\hat{\theta}) \tag{11}$$

and

$$C(t-\hat{\tau}-\Delta)\cos(29.25\omega t+\hat{\theta}) \tag{12}$$

where $\Delta$=1/2 chip. This technique is referred to as $\tau$-dithering. The feedback signal is at either the early or late position, represented by equations (11) or (12) respectively, for a period of 20 ms beginning at the start of each incoming data bit. Therefore the process controller requires a time interval corresponding two data bits (40 ms) to estimate the NDLL error term $\varepsilon_d$. This term is formed in the following manner

$$\varepsilon_d = EP-LP \tag{13}$$

where

$$EP = \left(\frac{1}{5}\sum_{k=1}^{5} I_k\right)_E^2 + \left(\frac{1}{5}\sum_{k=1}^{5} Q_k\right)_E^2$$

and

$$LP = \left(\frac{1}{5}\sum_{k=1}^{5} I_k\right)_L^2 + \left(\frac{1}{5}\sum_{k=1}^{5} Q_k\right)_L^2$$

The E and L indicate whether the feedback signal was in the early or late position, respectively. The determination of which measurement, early or late, is performed first is a random quantity. This prevents biasing of the error term $\varepsilon_d$ in the presence of periodically-pulsed jammers. The error term is updated every 250 ms, according to the sequence shown in Figure 9.

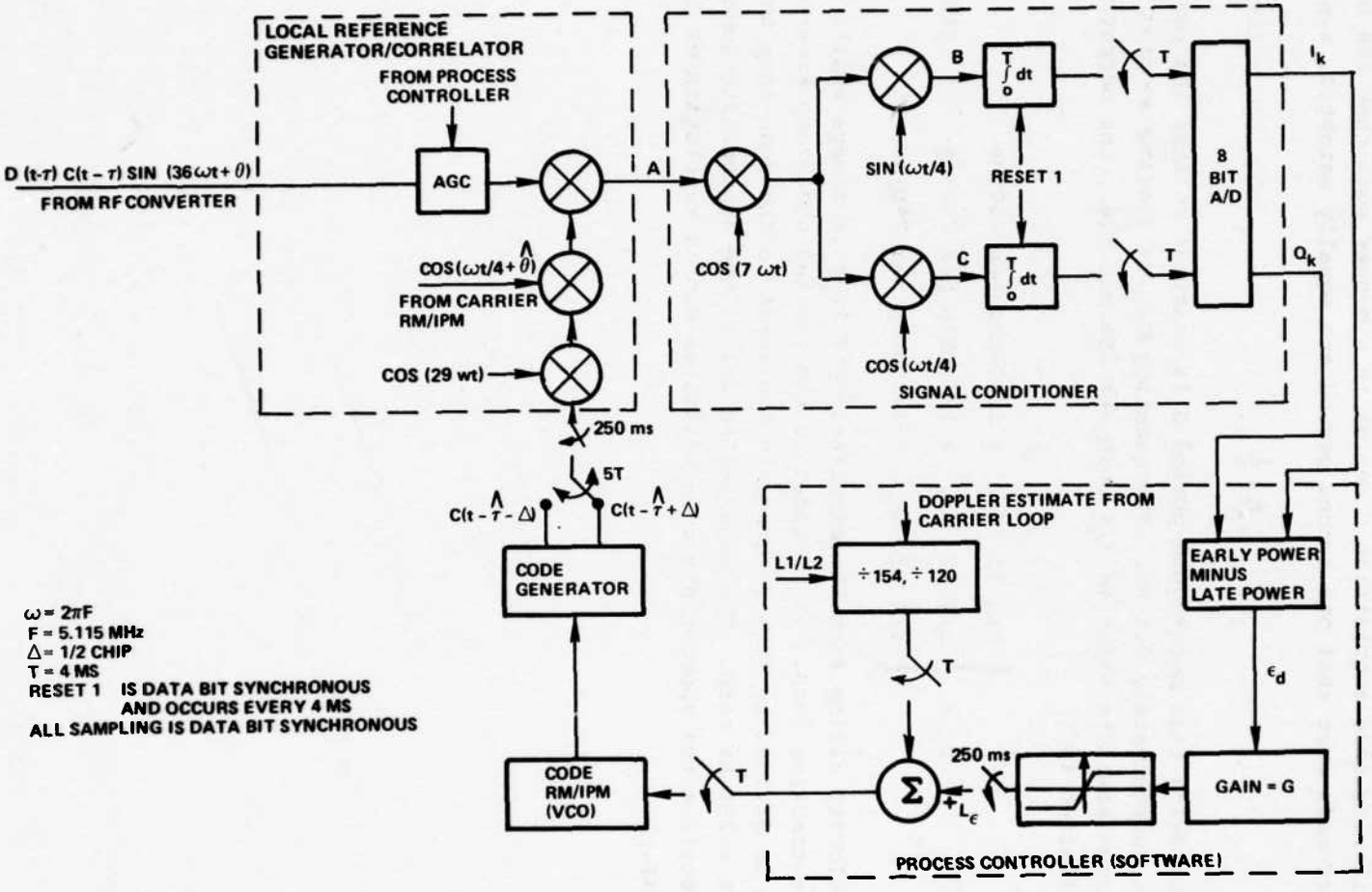


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Figure 20. X-Set Code Tracking Loop
From References [1-5]

The error is then multiplied by a gain, G. For the first one second following code acquisition G varies in a manner such that the measurements made over that one second period are equally weighted, i.e.,

$$G \alpha \frac{1}{t} \tag{14}$$

Following this one-second period G is constant so that the bandwidth is approximately 0.1 Hz. The quantity $(G\epsilon_d)$ is limited so that its maximum absolute value is 1/4 chip per 250 ms, i.e., the output $L_\epsilon$ of the limiter is

$$L_\epsilon = \begin{cases} G\epsilon_d \text{ if } |G\epsilon_d| \leq 1/4 \text{ chip per 250 ms} \\ 1/4 \text{ if } G\epsilon_d > 1/4 \text{ chip per 250 ms} \\ -1/4 \text{ if } G\epsilon_d < -1/4 \text{ chip per 250 ms} \end{cases} \tag{15}$$

Velocity aiding from the carrier-loop filter is always applied to the code-tracking loop. It is added to the limited code-loop error and the sum is divided by five to generate the input to the code-loop RM/IPM (VCO) at a 250 Hz rate. The code RM/IPM drives the appropriate generator which provides the appropriate code estimates with a resolution of 1/64 of a chip.

## Section 7. Hold-On-By-Your-Teeth (HOBYT)[1] Operation

The bandwidth of the Costas loop will generally be substantially greater than the bandwidth of the AFC loop, and the bandwidth of the AFC loop will generally be substantially greater than that of the code loop. Hence, as the jamming level increases, the Costas loop is the first to lose lock. When this happens, the receiver enters the Hold-On-By-Your-Teeth (HOBYT) mode, wherein it attempts to maintain code lock, utilizing IMU data or, if an IMU is not available, AFC/Costas data as an aid to code tracking. If the HOBYT mode fails to maintain code lock, the receiver retreats to the reacquisition mode, as described in Section 15. The jamming-to-signal ratio must return to a relatively low value, less than 34 dB, ($C/N_o$>36 dB-Hz), before the reacquisition mode will be successful [1,3].

If there is no IMU, when Costas loss-of-lock is sensed the AFC/Costas loop is enabled*. The receiver operates in this mode until loss-of-lock is indicated for the AFC/Costas loop. When AFC/Costas lock is lost then the receiver attempts to reacquire the signal.

If IMU data is available, when Costas loss-of-lock is sensed and the $C/N_o$ estimate is between 14 and 24 dB-Hz the Costas loop is disabled and the IMU is used to aid the code loop. IMU aiding is implemented by turning off the inputs to the carrier loop filter and stuffing the reformated line-of-sight acceleration and velocity data (from the IMU via the data processor) into the appropriate integration registers in the carrier loop filter. As before, the output of the carrier loop filter is used to aid the code loop. When the $C/N_o$ estimate is less than 14 dB-Hz the receiver starts a reacquisition process for that satellite signal.

The detailed criteria for entering and exiting from the various HOBYT configurations are specified in Figure 14 of reference [3].

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*See footnote on page 32.

## Section 8. Initial Acquisition Procedure

There are two methods by which a satellite signal may be acquired. In the normal acquisition mode the X-set receiver first acquires and tracks the Coarse/Acquisition (C/A) signal then switches to track the Precision (P) signal. The second acquisition method, called direct acquisition, acquires the P signal directly. Since the period of the P signal is very long (approximately 267 days) and the chip duration is very short (approximately 100 ns), direct acquisition requires precise knowledge of system time to within 1 second and a good estimate of the receiver velocity. On the other hand, because the C/A code has a short period (1 ms) and a long chip length (1μs), normal acquisition doesn't require apriori knowledge of system time or an estimate of receiver velocity.

The operations performed for normal acquisition are shown in Figure 21. Each of these operations is described in detail in other sections and will be discussed only briefly here. First the sequential detector uses all available channels (for the first signal to be acquired the code channel and all four carrier channels are used so that the average acquisition time is reduced by a factor of 5) to perform simultaneous code and frequency correlations (and incoherent power detections) using a single code delayed by different amounts. This procedure is repeated with different trial code delays and frequency estimates until substantial power is detected. Then one receiver channel concentrates on acquiring this signal while the remaining channels search for the next signal. A Noncoherent Frequency-Locked Loop (NFLL) pulls the frequency to within the range of the AFC/Costas loop, while a Noncoherent Delay-Locked Loop (NDLL) attempts to track the code delay. After 1 second the frequency and code pull-in mode switches to a frequency and code tracking mode. AFC/Costas loops and a NDLL are employed in this mode. When the carrier estimate is within the Costas loop range the AFC portion of the loop is disabled and the third-order Costas loop* and NDLL are used to track carrier phase and code delay, respectively. When Costas lock has been achieved the user-time clock is synchronized to the incoming data bits. (The user-time clock controls all of the receiver sampling and resets the integrators in the

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*See footnote on page 32.

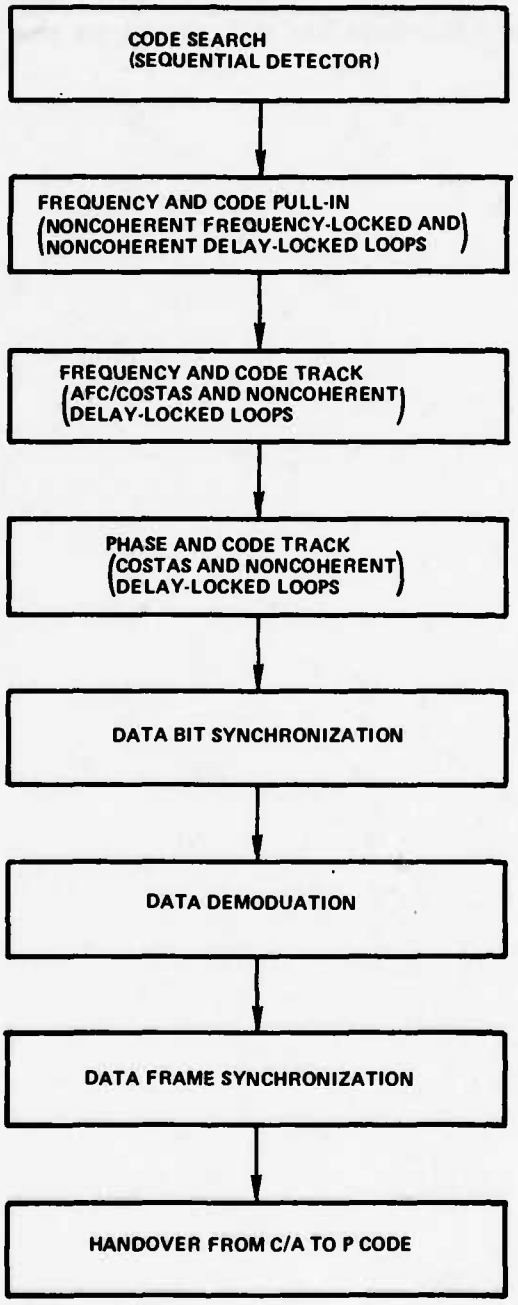


Figure 21. X-Set Acquisition Procedure for A Single Channel From References [1,3]

integrate-and-dump circuits). Next the process controller demodulates the data and identifies the next frame received. Using the received data, the handover function from the C/A signal to the P signal is initiated.

## Section 9. C/A Code Search

The C/A code search in the X-set is performed by the sequential detector. The sequential detector searchs in both time and frequency. A uniform-time distribution and a Gaussian-frequency distribution are assumed. The frequency search is centered about the pseudo-range rate estimate provided by the data processor. The magnitudes of the time and frequency uncertainties are also provided by the data processor. For initial C/A acquisition, these values are 1 ms and 800 Hz (1-$\sigma$), respectively.

The sequential detector performs a maximum-likelihood-ratio test on an approximation of the envelope of the received signal correlated with the current code and frequency settings. There are three regions in the ratio test; rejection, acceptance, and continue regions. If after a fixed number of samples, 128, the current code and frequency settings have not been rejected, the sequential detector assumes that the signal-envelope estimate is within the acceptance region. A functional block diagram of the sequential detector is shown in Figure 22. The inputs to the sequential detector are the one-millisecond inphase and quadrature samples, $I_k$ and $Q_k$, respectively. The envelope of the correlated signal is approximated by

$$\text{env} = |I_k| + |Q_k| \tag{16}$$

A bias is subtracted from the envelope approximation. The difference is accumulated, and after each sample the accumulation is compared with the rejection threshold. (As of this writing, the rejection threshold has not been determined). If the accumulation is below the rejection threshold the current code setting is rejected. The desired average number of samples $\bar{N}$ accumulated prior to rejecting a code setting is ten. If the current number of samples differs from this desired average by more than 25% the gain of the automatic gain control circuitry is appropriately increased or decreased by 1 dB. If this is not the case, a new bias value is determined. The new bias value is determined in the following manner

$$\text{bias} = \text{bias} + (N-10)/8 \tag{17}$$

Where N is the current number of samples taken prior to dismissal. N is then set to one and the contents of the accumulator zeroed. The code

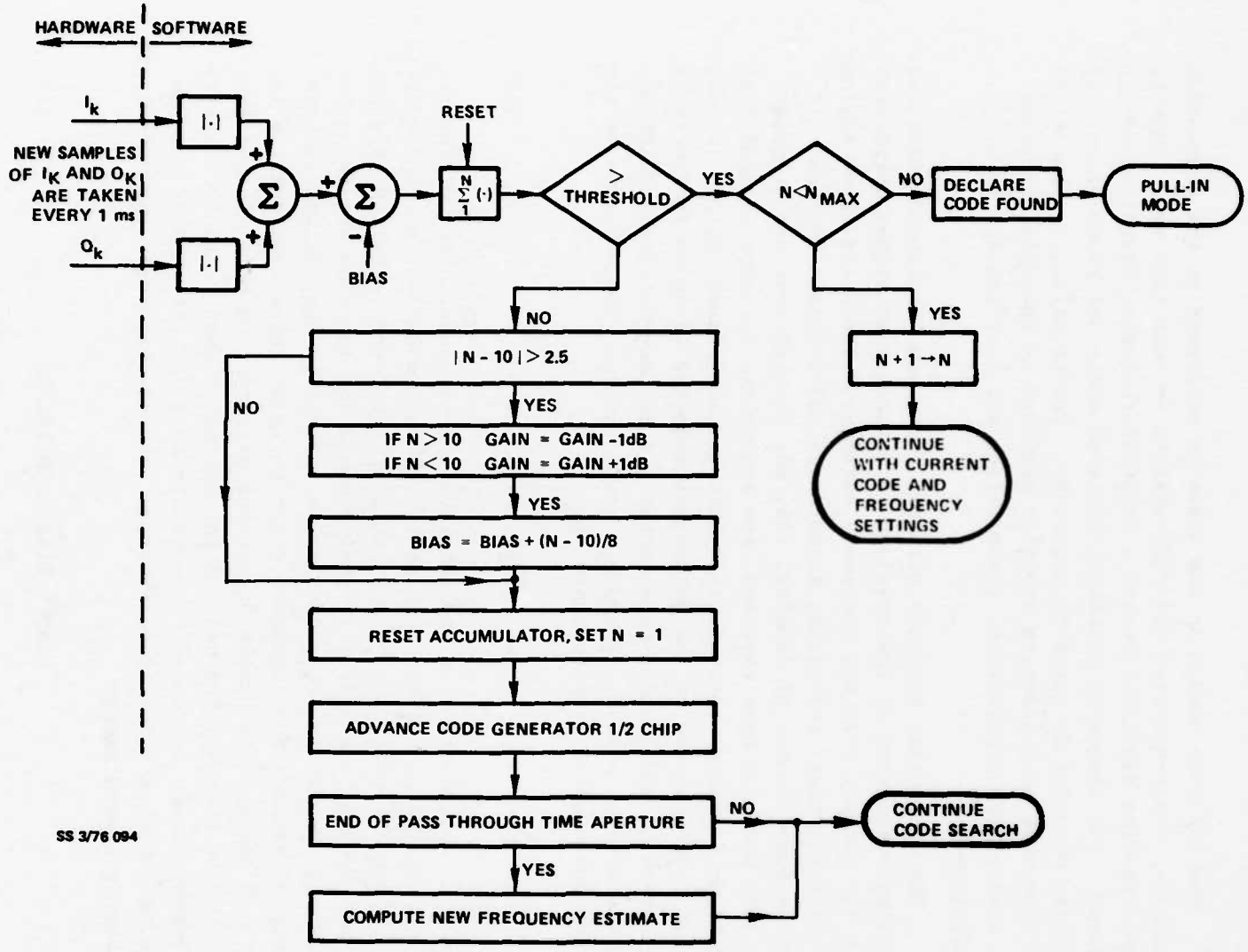


Figure 22. X-Set Code Search Operation
From References [1,3,8]

generator is then advanced by 1/2 a chip. After the sequential detector advances the code generator, it determines whether it has completed a pass through the time aperature. If it has, a new frequency estimate is computed and the process is repeated with the new frequency and code estimates. If not, the process is repeated with the current frequency estimate and the new code estimate.

However if the accumulation of the envelope estimates minus bias terms is greater than the rejection threshold, the number of samples in the accumulation is tested to see if it is less than the maximum number of samples, $N_{max} = 128$, that must be taken before code acquisition is tentatively declared. If N is less than 128, N is incremented and the process continues. If not, tentative code acquisition is declared and the receiver enters the Pull-In mode.

## Section 10. Pull-In Mode

After the sequential detector tentatively declares that the code has been found, the X-set receiver enters the Pull-In mode. In this mode the receiver attempts to pull the frequency within the range of the AFC/Costas loop and to pull-in the code. The noncoherent delay-locked loop previously discussed is used for code pull-in. A first-order Noncoherent Frequency-Locked Loop (NFLL) operating for a predetermined time interval, 1 second, is employed to generate an estimate of the carrier frequency. At the end of the time interval the receiver switches to the AFC/Costas loop and the AFC lock indicator is monitored. If after 1 second the indicator fails to indicate lock, false code lock is declared and the code search mode is reentered. However if AFC lock is obtained, the AFC/Costas loop and the NDLL are used to track the frequency and code, respectively.

The implementation of the NFLL and associated logic is shown in functional block diagram form in Figure 23. The feedback signal is alternately switched every 20 ms between

$$C(t-\hat{\tau})\cos[(MF+450)2\pi t]$$

and (18)

$$C(t-\hat{\tau})\cos[(MF-450)2\pi t]$$

where MF is the frequency estimate of the NFLL. The one-millisecond inphase and quadrature samples are used to form estimates, PU and PL, of the power in the upper and lower frequencies. The next frequency estimate is formed in the following manner

$$MF_n = MF_{n-1} + C_9(PU-PL) \tag{19}$$

where $C_9$=0.6 for the first four 40-ms samples and 0.2 thereafter. Then, based upon the logic in Figure 23, the receiver decides to continue in the pull-in mode, reenter the code search mode, or track the frequency and code with the AFC/Costas loop and NDLL, respectively.

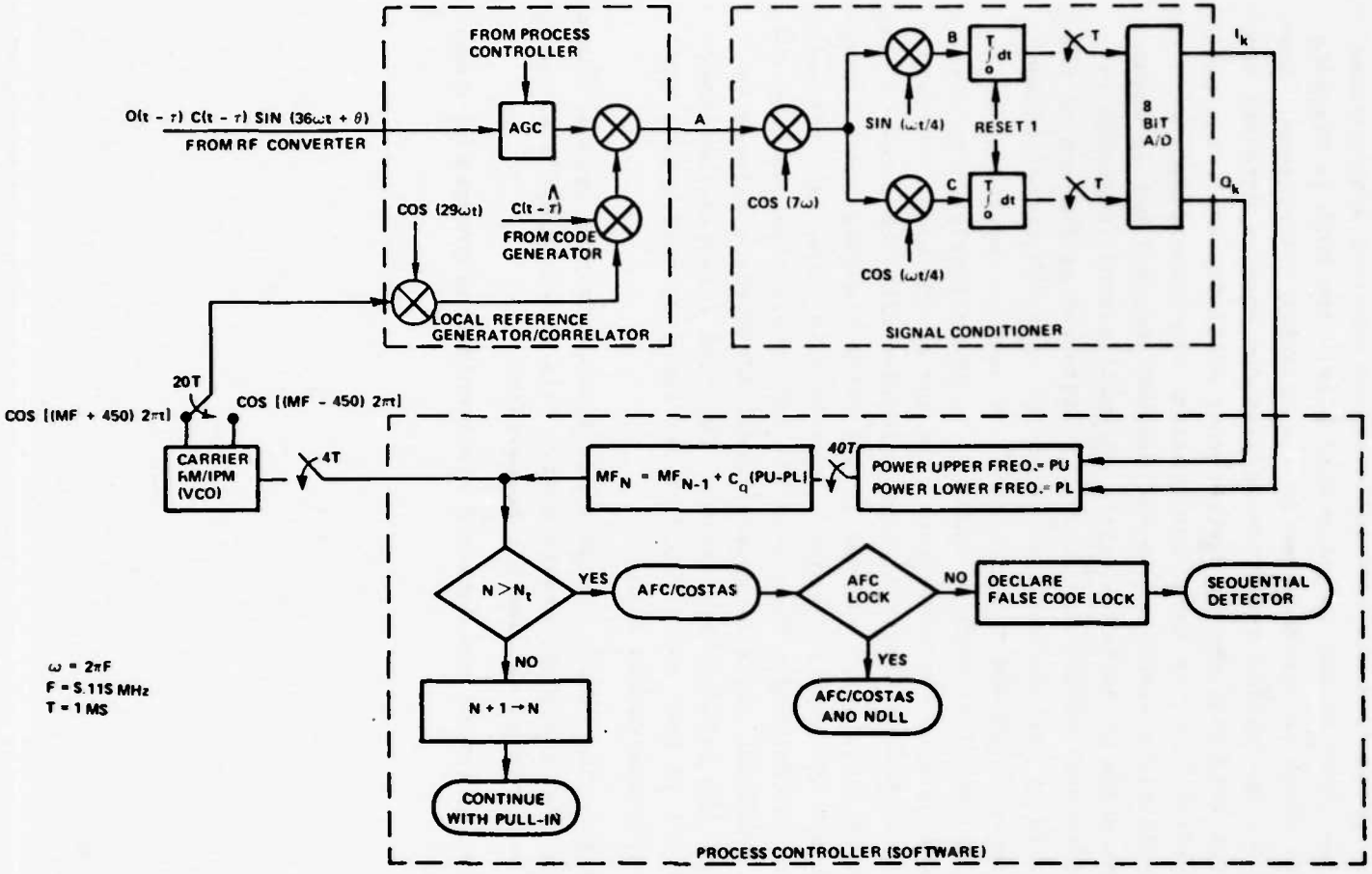


Figure 23. Noncoherent Frequency-Locked Loop Used In X-Set Receiver For Frequency Pull-In From References [1,3]

## Section 11. Data-Bit Synchronization

After Costas lock has been achieved the receiver synchronizes the user-time clock to the incoming data bits. The NDLL is tracking the C/A code which is synchronized to the data-bit transitions. However the C/A code repeats every one millisecond whereas data-bit transitions occur less frequently, every twenty milliseconds. Thus using only information from the NDLL, the receiver can accurately locate the data-bit transitions within a one-millisecond interval but is unable to determine which of twenty possible one-millisecond intervals in which the data-bit transition occurs. A histogram of the sum of the sign reversals of the inphase samples of the received signal in each of twenty one-millisecond time intervals is used to resolve this ambiguity. One second of inphase samples (or equivalently fifty data bits) is used to form the histogram. The sum of the sign reversals in the one-millisecond interval which coincides with the data-bit transition must be larger than the sum in any other one-millisecond interval by at least ten sign reversals. When this is true, data-bit synchronization is declared. When data-bit synchronization has been declared the user-time clock is appropriately advanced or delayed to coincide with the data-bit transition. Then the integrate-and-dump interval is set to four milliseconds. The receiver then enters the data-frame synchronization mode.

If at any time during the data-bit synchronization process Costas lock is lost, the procedure starts over.. This prevents cycle skipping from being interpreted as data-bit transitions.

A flow diagram of the data-bit synchronization process is shown in Figure 24.

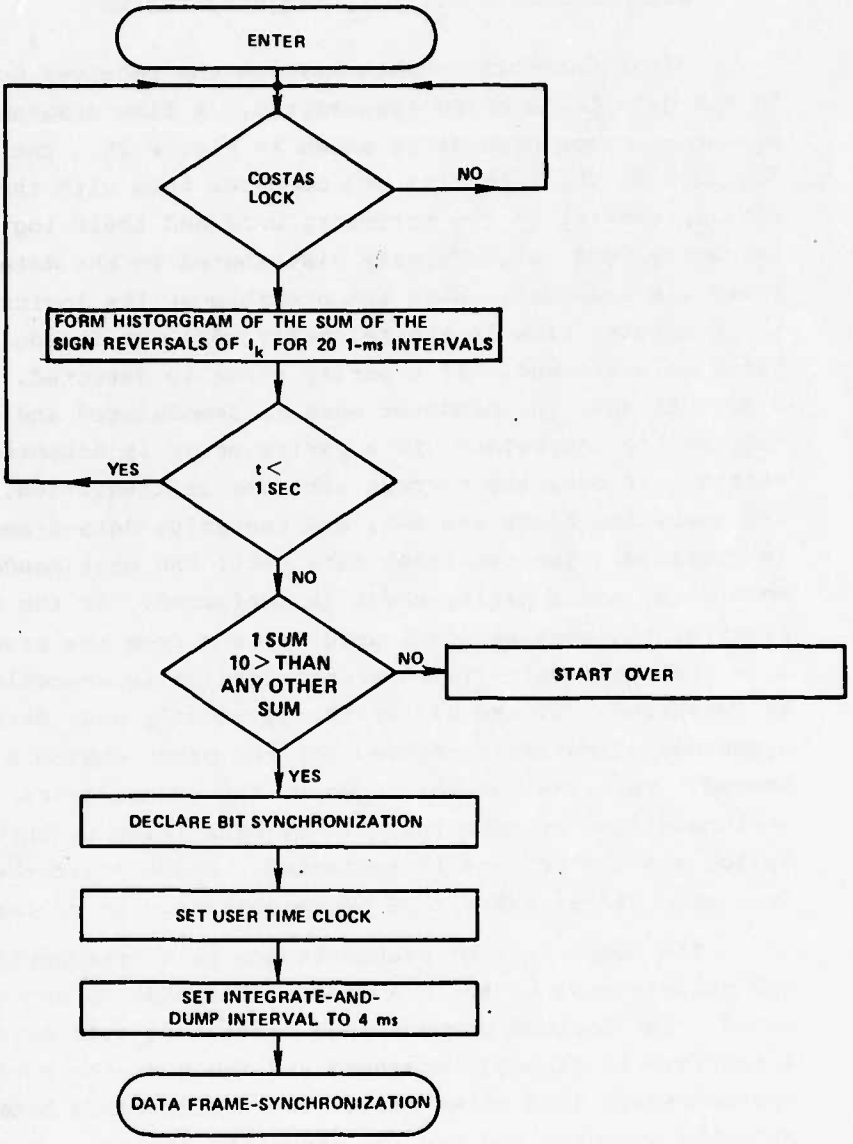


Figure 24. X-Set Data-Bit Synchronization Procedure From References [1,3]

## Section 12. Data-Frame Synchronization

After data-bit synchronization the receiver must be synchronized to the data frame being transmitted. A flow diagram of the data-frame synchronization process is shown in Figure 25. The process controller demodulates the data bits and compares them with the synchronization bits (preamble) of the telemetry word and their logical inverse. (The telemetry word is uniformily distributed in the data frame and occurs every six seconds). When the preamble or its logical inverse is detected the remaining bits in the telemetry word are demodulated and a parity check is performed. If a parity error is detected, the process starts over. If not, the handover word is demodulated and a parity check is made on it. As before, if a parity error is detected the process restarts. If not, the current subframe is identified, the pseudo-range and user-time clock are set, and tentative data-frame synchronization is declared. The remaining data until the next handover word is demodulated, and a parity check is performed. If the Z-count (system time) of the next handover word differs from the previous Z-count by more than one, data-frame synchronization is cancelled and the procedure is restarted. If the difference is exactly one, data-bit and data-frame synchronization are performed for the other channels that are Costas locked. Then the pseudo-ranges of the channels are compared. If any of them differ by more than 21 ms, data-frame synchronization is cancelled and the process is restarted. However, if the differences are less than 21 ms, data-frame synchronization is declared.

The comparison of pseudo-ranges is a reasonability test. Twenty-one milliseconds of the C/A code corresponds to approximately 4000 miles. The maximum pseudo-range difference will exist when one of the satellites is directly overhead and one near the horizon. There is approximately 4000 miles pseudo-range difference between a satellite directly overhead and one 15° above the horizon. Normally satellites with elevation angles lower than 15° above the horizon will not be used for navigation. Thus, if the pseudo-range difference is greater than 4000 miles the user-time clock has probably been incorrectly set and the data-frame synchronization process (which sets the user-time clock) is repeated.

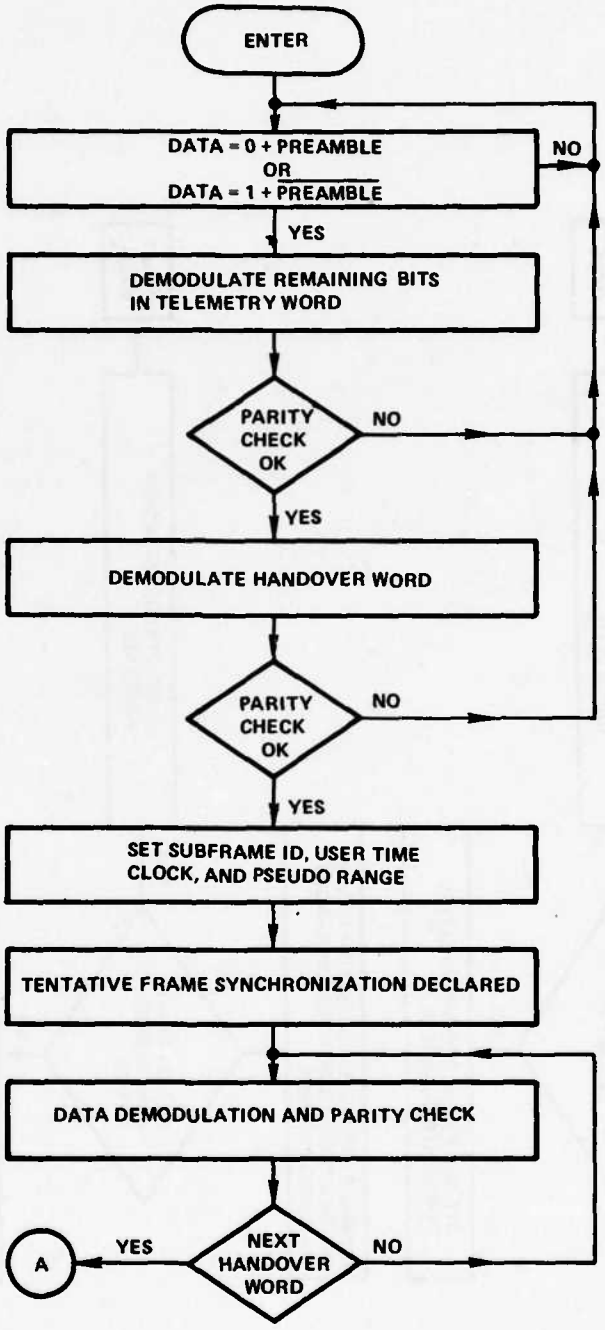


Figure 25. X-Set Data Frame Synchronization
From Reference [3]

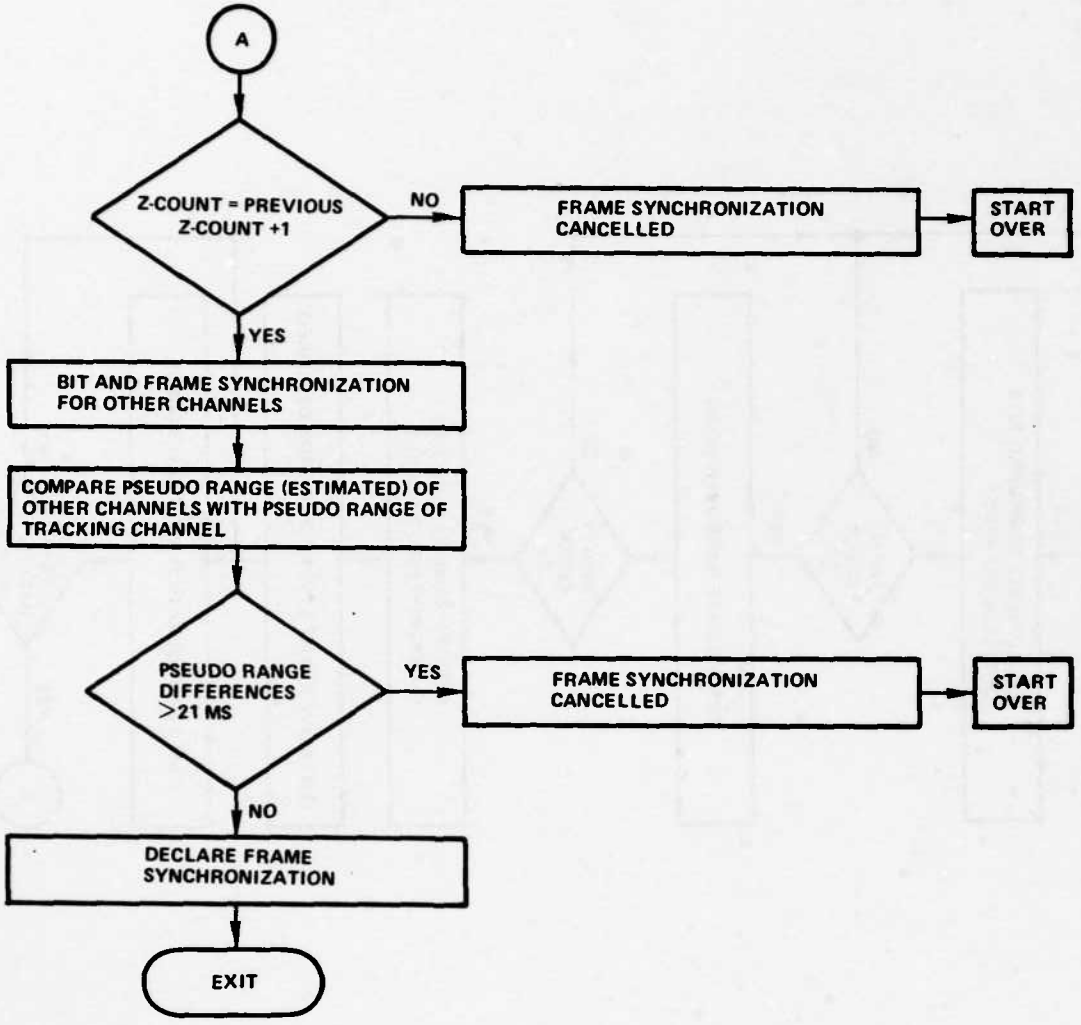


Figure 25. X-Set Data Frame Synchronization (Continued)
From Reference [3]

## Section 13. Handover Function

After data-frame synchronization and handover word demodulation, system time is known unambiguously. Thus the P-code generator for that channel can be appropriately set and the handover from the C/A signal to the P signal completed. Figure 26 is a flow diagram of the X-set handover procedure. First the receiver looks for the sixth word of the current subframe. At the start of the sixth word the receiver sets the X1 register in the P-code generator at the beginning of its epoch. The P-code generator is then slewed to the proper time-of-week in 1.5-second increments. This requires a maximum of 1.62 seconds. While this operation is occuring, the receiver continues to track the C/A signal. Then the P-code is advanced five chips and at the beginning of the next telemetry word, a narrow-aperature reacquisition procedure is used to acquire the P signal. Advancing the P code five chips helps prevent the code loop from locking on a multipath signal.

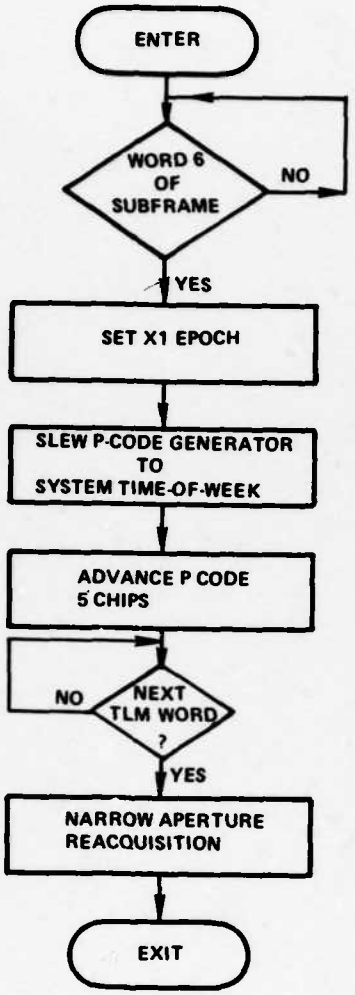


Figure 26. X-Set Handover From C/A to P Signal Procedure From Reference [3]

## Section 14. Data Demodulation

After data-frame synchronization is complete the process controller demodulates and reformats the incoming data words for transfer to the data processor. A functional flow diagram of the data demodulation process is shown in Figure 27. The four-millisecond inphase samples from the Costas loop are summed over a data bit and the sign of the sum is used to determine the incoming data bit. If the sum is negative then the data bit is a "one" and if the sum is positive then the data bit is a "zero". The last bit demodulated is appended to the current data word. This operation continues until the data word is complete. There are thirty bits per data word. When the word is complete the process controller checks the parity of the current data word. The process controller also checks to see if the receiver maintained Costas lock while demodulating the current data word. Then the parity-okay bit and demodulator working bit, which indicates whether Costas lock was maintained or not, are properly set and the word is transferred to the data processor. The process controller proceeds to demodulate subsequent data words.

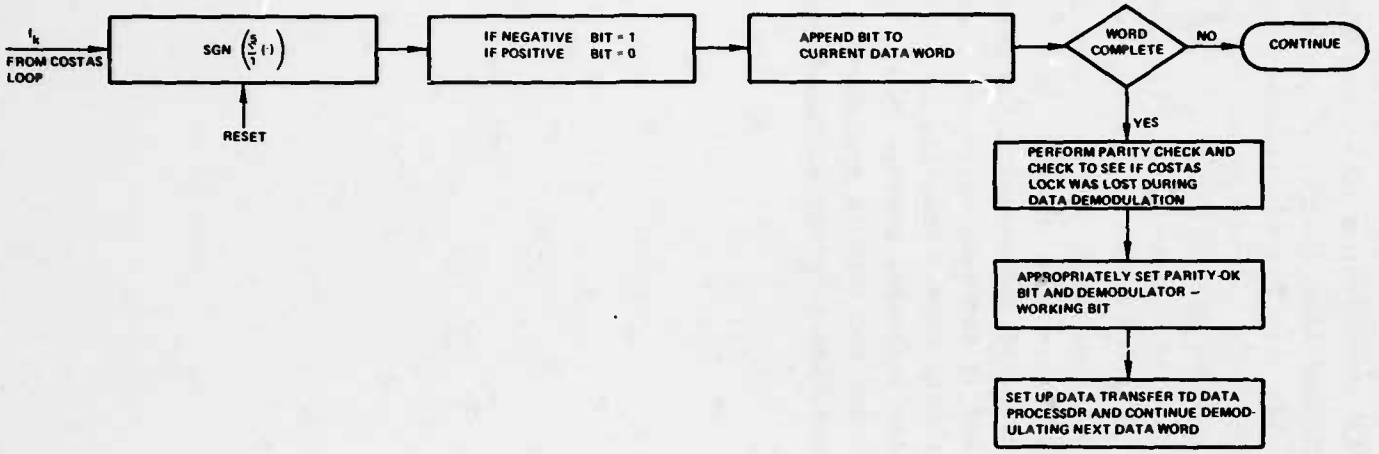


Figure 27. X-Set Satellite-Data Demodulation Process
From Reference [3]

## Section 15. Reacquisition Procedure

If for a short period of time the X-set receiver loses both carrier and code lock on a channel, the receiver enters a reacquisition mode. The reacquisition procedure is shown in flow diagram form in Figure 28. The reacquisition procedure may be performed using either the C/A code or the P code. First the acceleration uncertainty $\sigma_{acc}$ is determined. Then the time and frequency search aperatures are determined as a function of the acceleration uncertainty

$$\text{time search aperature} = C_{10}\sigma_{acc}t^2 \qquad (20)$$

$$\text{frequency search aperature} = C_{11}\sigma_{acc}t \qquad (21)$$

Where t is the elapsed time from signal loss. At the time of this writing, design values for $C_{10}$ and $C_{11}$ had not been determined. If the search aperature growth rate is excessive the receiver is forced to the C/A acquisition mode with maximum time and frequency uncertainties. If the growth rate is not excessive the sequential detector searches for the code in the aperature just calculated. If the code is not found a new search aperature is calculated and the operations described above continue until the C/A acquisition mode is entered or the code is found. When the code is found the receiver enters the pull-in mode. After 1 second the receiver switches to the AFC/Costas loop for carrier acquisition. If after 1 second lock is not indicated, new search aperatures are determined and the process is repeated. If AFC lock is achieved, the receiver declares signal reacquisition and tracks the code with the NDLL and the carrier with the AFC/Costas loop or the Costas loop*.

The procedure used to determine the acceleration uncertainty is shown in Figure 29. If an IMU is aiding the receiver, the acceleration uncertainty is set to 0.1 $m/sec^2$. If not, and if no channels are Costas locked then the acceleration uncertainty is set to 1 $m/sec^2$. If the receiver is not IMU aided and at least one channel is Costas locked then the acceleration uncertainty is:

$$\sigma_{acc} = \text{minimum of } (n \cdot a_{max}, 30)\, m/sec^2 \qquad (22)$$

where n is the number of channels not Costas locked and $a_{max}$ is the maximum acceleration indicated on any of the channels that are Costas locked.

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*See footnote on page 32.

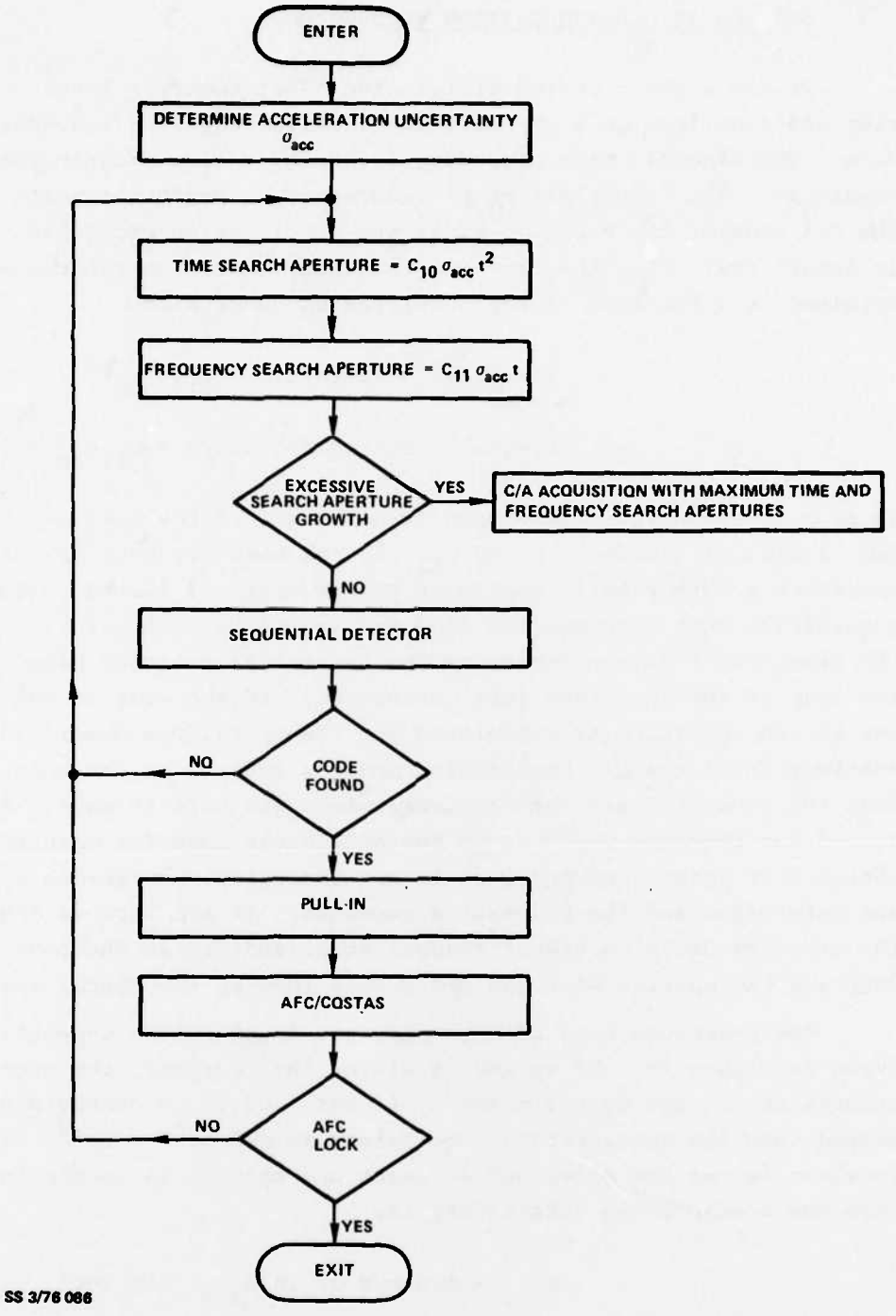


Figure 28. X-Set Reacquisition Procedure From Reference [3]

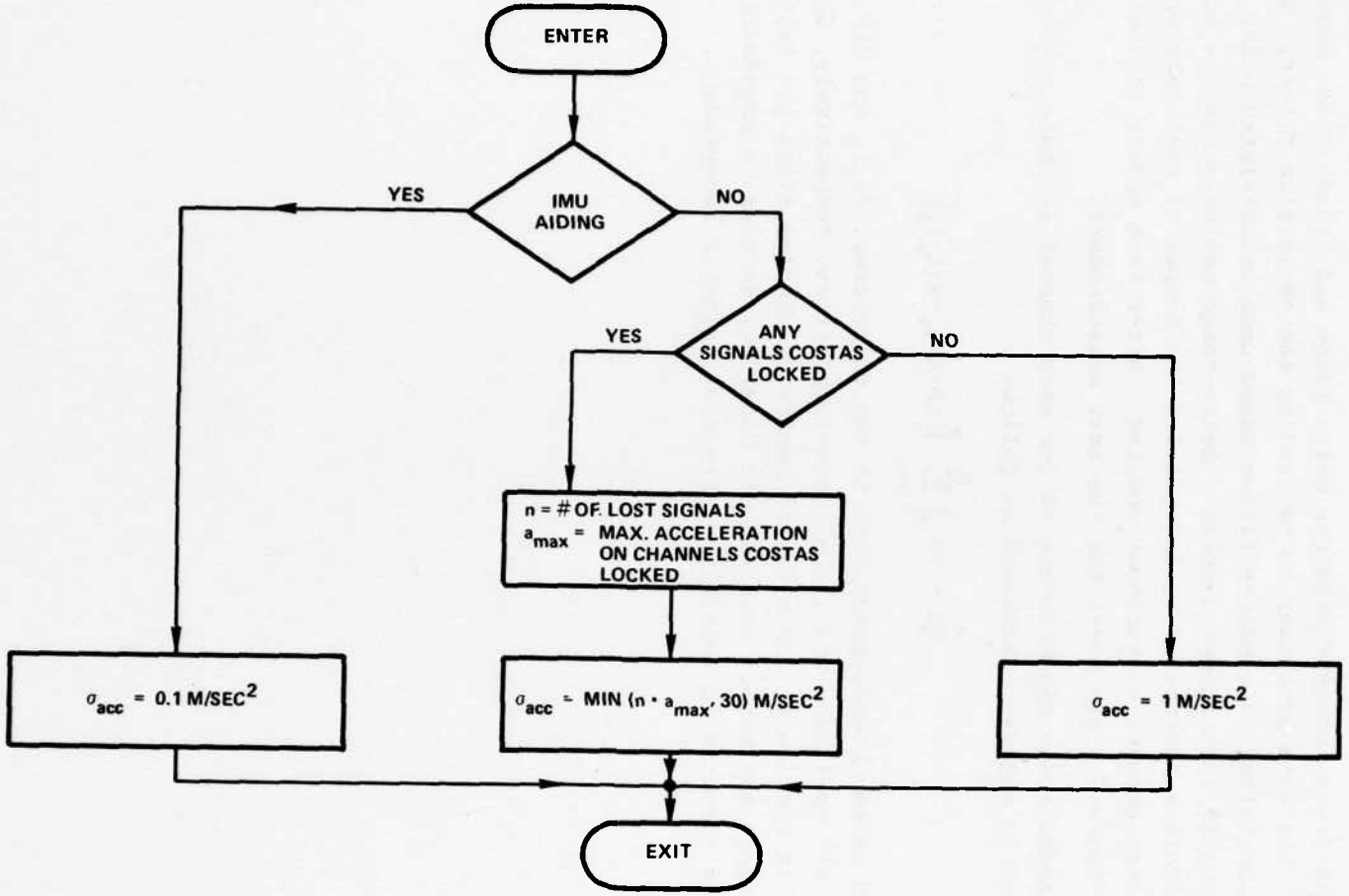


Figure 29. Acceleration Uncertainty Determination For X-Set Reacquisition Procedure From Reference [3]

## Section 16. Delta-Range and Pseudo-Range Measurements

The X-set receiver provides delta-range and pseudo-range measurements to the data processor to be used in the navigation filter. The navigation filter is a Kalman filter based upon uncorrelated noise and statistically independent samples. Delta-range measurements are made in the process controller by integrating the output of each carrier loop filter between measurement updates. After each update the delta-range integrators are reset for the next measurements.

Pseudo-range measurements PR for each channel are made as shown in Figure 30 and are calculated as follows

$$\widehat{PR} = PR + \frac{1}{N} \sum_{k=1}^{N} \left[ (EP\text{-}LP)_k - k(L_\varepsilon)_k \right] \qquad (23)$$

where PR is the pseudo-range seen at the correlator, $(L_\varepsilon)_k$ and $(EP\text{-}LP)_k$ are the $k^{th}$ nonlinear and linear code-loop errors, respectively, described in section 6, and N is the number of samples since the last pseudo-range estimate. According to Magnavox, successive pseudo-range estimates computed in this manner are statistically independent.

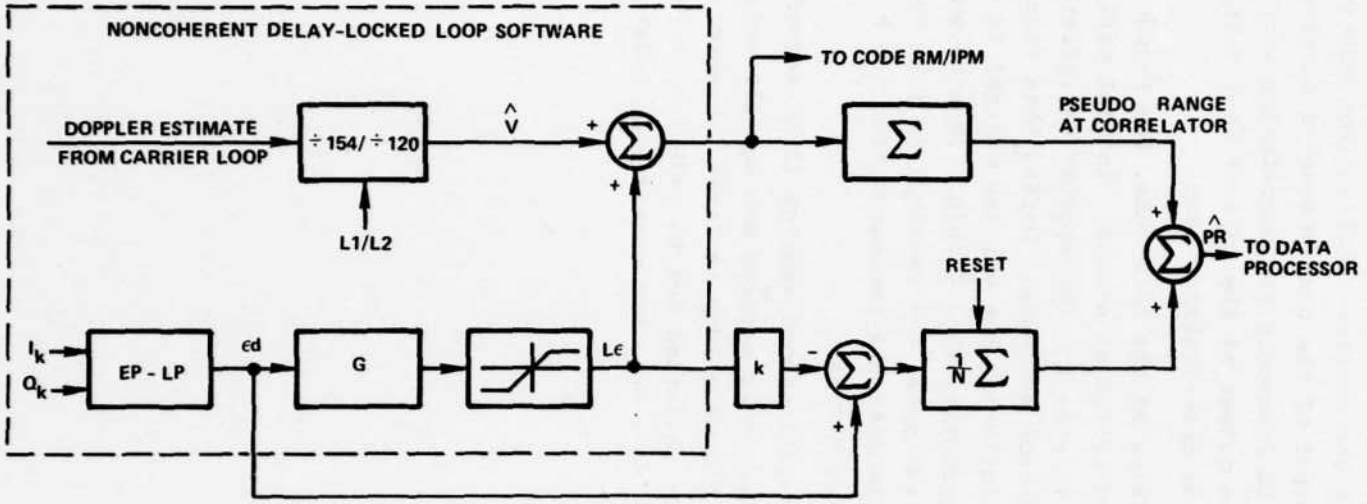


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Figure 30. X-Set Pseudo-Range Measurement
From Reference [3]

## Section 17. L1-L2 Measurements

To make L2 measurements the code tracking loop is switched to track the L2 signal. However the carrier-tracking loop continues to track the L1 signal. The output of the code channel's carrier RM/IPM (VCO) is scaled down to the L2 frequency for correlation with the L2 signal in the code loop. The output of the carrier loop filter is also properly scaled for aiding the code-tracking loop.

To initialize the tracking of the L2 P code, the P-code estimate from the L1 signal is delayed by 1/2 of a chip. Initial early/late measurements are made about this point. Subsequent early/late measurements are made from the L2 P-code estimate. During this time, the L1 code estimate used for correlation in the carrier channel is slightly perturbed. The maximum perturbation is $\pm \frac{1}{4}$ chip. Thus by subtracting the L2 estimate from the L1 estimate, the receiver is able to measure the difference between the pseudo-range estimates from the P codes received on the L1 and L2 frequencies.

For the first 160 four-millisecond samples (0.64 seconds) all of the code-loop inphase and quadrature samples are equally weighted. After that the bandwidth of the code loop is fixed. However as before, the maximum code RM/IPM (VCO) variation due to code loop error is constrained to be less than 1/4 of a chip per measurement update.

## Section 18. Automatic Gain Control

The process controller controls the Automatic Gain Control (AGC) circuitry in the local reference generator/correlator. There are five different modes of AGC operation. In each of the modes the AGC adjustment has a first-order response with a 1 dB resolution. A general block diagram of the AGC loop is shown in Figure 31. The process controller uses the inphase and quadrature samples $I_k$ and $Q_k$ from the signal conditioner to form the measurement used for AGC control. It generates the AGC loop error by subtracting the nominal (desired) measurement value from this measurement. This difference is accumulated as in a perfect integrator and divided by the loop time constant $\tau$. The integer portion of this value is sampled and used to appropriately set the AGC gain. Tha adjustment interval, time constant, and the measurement which is the basis for AGC adjustments differ between modes.

Initially the AGC must be set so that upon entering the code search mode the sequential detector will operate properly. The AGC is initialized in the following manner. The incoming signal is correlated with a random setting of the P-code generator and the nominal carrier frequency. The input to the AGC loop is the sum of the absolute values of the inphase and quadrature samples, i.e.,

$$|I|_k + |Q|_k \tag{24}$$

Since there is no attempt at code alignment in this mode, Equation 24 is an estimate of the noise envelope. The gain is adjusted every four milliseconds and the loop time constant is 0.2 seconds. The receiver stays in this mode for at least one second. This allows the gain to settle to its proper value before proceeding to the code search mode.

While in the code-search mode the gain is set so that the sequential detector maintains a constant search rate. The manner in which the gain is controlled is described in Section 9 which discusses the sequential detector.

Equation (24) is also the AGC measurement in the frequency pull-in mode, Section 10. However, depending upon the acquisition mode, normal or direct, the incoming signal is correlated with either the C/A code or the P code, respectively. In this mode, Equation (24) is an estimate of the envelope of the signal plus noise. The time constant of the AGC loop is 0.1 second and the gain is adjusted every thirty-two milliseconds.

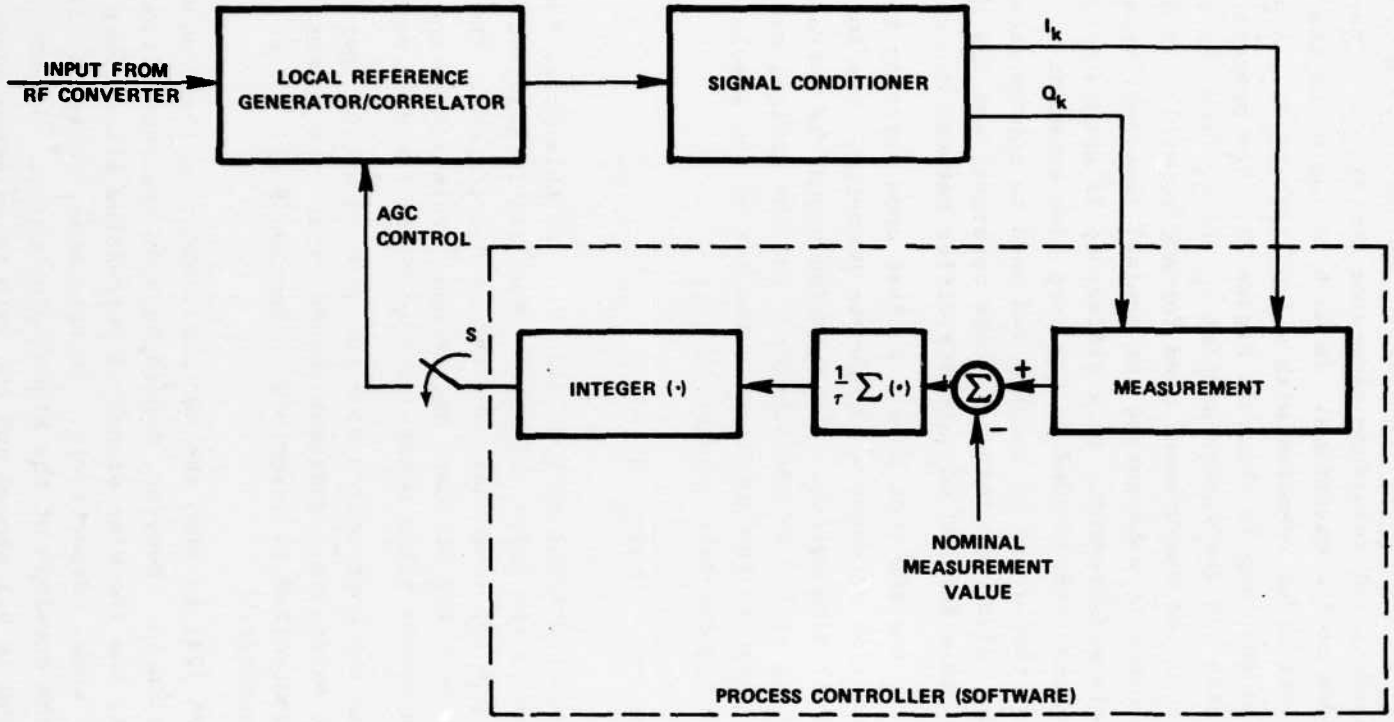


Figure 31. X-Set Automatic-Gain Control Loop From References [1,3,5].

There are two cases to consider when the carrier and code are being tracked. In the first case, the automatic-frequency-control loop is locked to the incoming signal but the Costas loop is not. Then Equation (24) is again the AGC loop input. If Costas lock has been achieved, gain settings are determined from the absolute value of the inphase samples, which are coherent estimates of the signal amplitude. In both cases the gain is adjusted every four milliseconds and the AGC time constant is one second. Except when L2 measurements are being made, the AGC setting of the code channel is the same as the AGC setting of the carrier channel associated with the current code-error measurement. When L2 is being measured the code channel AGC is set 3 dB above the associated carrier channel AGC. (The L2 transmitted power is 3 dB less than the L1 transmitted power).

When the receiver is not locked on the carrier and IMU aiding is available, the AGC loop input is narrow-band power (NBP) minus wide-band power (WBP) where:

$$NBP = \left( \sum_{k=1}^{5} I_k \right)^2 + \left( \sum_{k=1}^{5} Q_k \right)^2 \tag{25}$$

and

$$WBP = \sum_{k=1}^{5} \left( I_k^2 + Q_k^2 \right) \tag{26}$$

The AGC loop time constant is ten seconds and the gain setting is adjusted every forty milliseconds.

## Section 19. List of References


1. Briefing charts presented at the NAVSTAR Global Positioning System Phase I Set X Unaided Critical Design Review, Magnavox Research Laboratory, 22-23 October 1975.

2. Rough draft of the "Computer Program Development Specification for the Set X Signal Processing Software X-SPS of the NAVSTAR GPS User Equipment Segment Phase I", CP-US-300, 24 October 1975, Received from J. Luse of SAMSO 10 February 1976.

3. Draft of the "Prime Item Development Specification for the GPS X-Receiver of the NAVSTAR GPS User Equipment Segment Phase 1," CID-US-101, 23 June 1975. Included as appendices are the following. "Simulation of the GPS Delay-Lock Receiver with IMU Aiding," C.R. Cahn, MRL Reference No. MX-TM-3176-75. "Threshold Reduction of GPS Receiver by IMU Aiding," C.R. Cahn, MRL Reference No. MX-TM-3175-75. "Alert Algorithm Design Specification," D. Knight, Magnavox Design Bulletin No. 0-15. "A Composite AFC/Costas Loop for Transition Between Frequency and Phase Tracking," C.R. Cahn, MRL Reference No. MX-TM-3165-75. "Sequential Detection Test for GPS C/A Acquisition," D. Leimer, MRL Reference No. MX-TM-3166-75. "Acquisition Time and Search Strategy for the GPS C/A - Signal Initial Acquisition," T. Tilk, MRL Interoffice Communications.

4. "A Proposal to SAMSO/JPO for the NAVSTAR Global Positioning System User System Segment," Vol. 2., General Dynamics, 12 June 1974.

5. Technical discussions with the GPS JPO and Aerospace Inc., 17-19 February 1976. Arranged by J. Luse of SAMSO.

6. Technical discussions with the GPS JPO and Aerospace Inc., 24 and 25 May 1976. Arranged by J. Luse of SAMSO.

7. Technical discussions with the GPS JPO, Aerospace Inc., and Magnavox Research Laboratory, 20-22 June 1976.

8. J. Luse, "X-Set Functional Description," letter to William Stonestreet, 19 October 1976.